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An integrated relative humidity sensor /

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AN INTEGRATED RELATIVE HUMIDITY SENSOR

by

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Table of Contents

Abstract 1

1. Introduction 2

1.1 Historical Background 2
1.2 Purpose of the Work 9

2. Theory of Circuit Operation 11

2.1 Sensor Theory 11
2.2 Measuring Circuit Theory 20

3. Design and Fabrication 32

3.1 Sensor Structure 32
3.2 Reference Capacitor Structure 32
3.3 Process Design 35
3.4 Layout 37
3.5 Fabrication 38

4. Testing and Evaluation of Results 39

4.1 Testing 39
4.2 Results 41
4.3 Conclusions 47
4.4 Recommendations 47

References 48

Appendix A. Two Phase Non-Overlapping Clock 51

A.1 General Circuit 51
A.2 Multivibrator 52
A.3 D Filp-Flop 52
A.4 Logic Stage 52

Appendix B. Example of SUPREM 58

Appendix C. A List of the Process Function and Layout for Each Mask Level 59

Vita 63

List of Figures

Figure 1-1:	Closed Volumes A, Which is Saturated with Water, and B Containing Water in an Unsaturated State	**2**
Figure 1-2:	Basic Structure of a Capacitive Hygrometer	**4**
Figure 1-3:	Aluminum Oxide Sensor (a) Structure and (b) Equivalent Circuit	**6**
Figure 2-1:	Basic Humidity Sensitive Capacitor	**12**
Figure 2-2:	Structure of the HyCal Humidity Sensor	**17**
Figure 2-3:	Normalized Humidity Response of HyCal Humidity Sensor	**19**
Figure 2-4:	Capacitance Measuring Circuit for the Integrated Relative Humidity Sensor	**21**
Figure 2-5:	Two Phase Non-Overlapping Clock Signal	**22**
Figure 2-6:	Switched Capacitor, (a) Conceptual, (b) Two Transistor Implementation, (c) Transmission Gate Implementation	**23**
Figure 2-7:	Condition of the Charge Balance Stage During (a) Phase 1, and (b) Phase 2	**25**
Figure 2-8:	Comparator Stage	**27**
Figure 2-9:	Integrator Stage	**28**
Figure 3-1:	Sensing Element Structure	**33**
Figure 3-2:	Reference Capacitor with Polyimide Dielectric	**34**
Figure 3-3:	Reference Capacitor with Silicon Dioxide Dielectric	**36**
Figure 4-1:	Saturated Salt Solution Apparatus	**40**
Figure 4-2:	Measurement of the Output of a Silicon Dioxide Reference Capacitor Humidity Sensor, First Run	**42**
Figure 4-3:	Measurement of the Output of a Silicon Dioxide Reference Capacitor Humidity Sensor, Second Run	**43**
Figure 4-4:	Output of the Sensor with Polyimide Reference Capacitors When Measured in "Pulsed" Mode	**45**
Figure 4-5:	A.C. Output of the Sensor	**46**
Figure A-1:	Non-Overlapping Clock Circuit	**51**
Figure A-2:	Multivibrator Circuit, (a) Actual Circuit, (b) Equivalent Circuit	**53**
Figure A-3:	D Flip-flop	**54**
Figure A-4:	Logic to Create Two Phase Non-Overlapping Clock	**55**
Figure A-5:	Clock Signals of the Two Phase Non-Overlapping Clock	**57**

List of Tables

Table 1-1:	Some Properties of Dupont's Fully Cured Polyimide Film	8
Table 1-2:	A List of Some Integrated Sensors Under Development	8
Table 1-3:	Circuit Functions in Integrated Sensors	9
Table 2-1:	Operating Characteristics of HyCal's Capacitive Humidity Sensor	18
Table 2-2:	Summary of Circuit Operation	31
Table 4-1:	Relative Humidities of Various Saturated Salt Solutions	41
Table A-1:	State of Nodes of Two Phase Clock Generating Circuit During 1 Cycle	56

Abstract

An integratred relative humidity sensor has been designed and produced. The sensor incorporates a capacitive sensing element with a measuring circuit implemented in CMOS technology.

The sensing element uses a polyimide dielectric whose permittivity varies with ambient relative humidity. A number of authors have investigated the moisture properties of polyimides with particular interest in the effect of moisture on permittivity. The results of several studies are considered here. One study has found the functional relationship between permittivity and ambient relative humidity to be nearly linear. An example of a discrete capacitive humidity sensor with a polymer dielectric is presented.

A capacitance measuring circuit that converts the sensing element's capcitance to a voltage output was designed. The circuit incorporates two reference capacitors to set the output voltage's gain and offset.

Two alternate structure designs were considered and processes were designed to place the sensing element on the same chip as the measuring circuit using both designs for comparison.

Sensors using both designs have been produced. Preliminary testing indicates that at least one sensor design is functional.

Chapter 1
Introduction

1.1 Historical Background

The development of an integrated relative humidity sensor results from work done in two fields of endeavor. The first field is the evolution of capacitive relative humidity sensors. The second field is the evolution of integrated or smart sensors.

Gregory and Rourke's text on hygrometry [9] provides a definition of the concept of relative humidity which I will use in this paper. Consider two closed volumes, *A* and *B*, as shown in Figure 1-1.

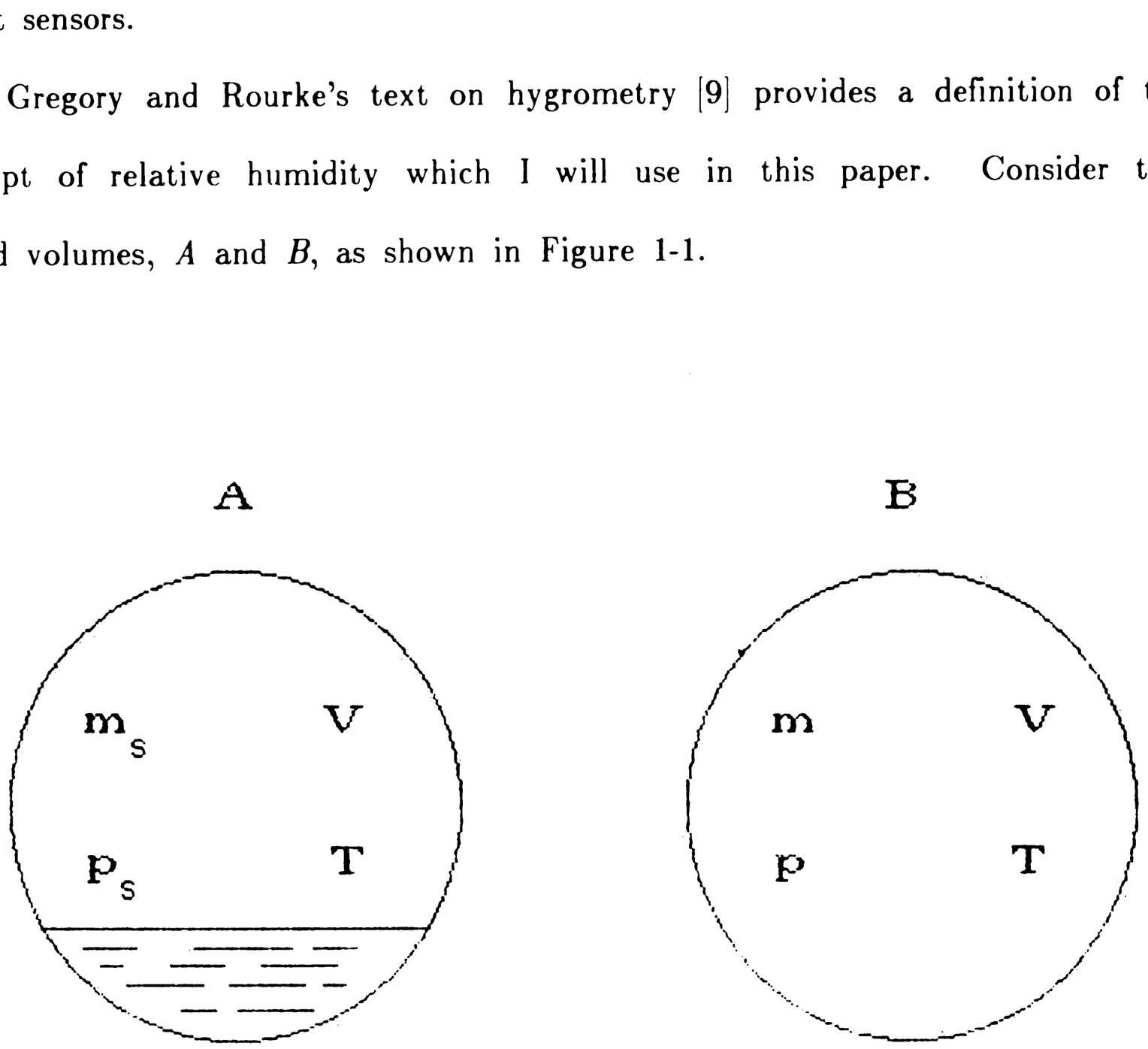


Figure 1-1: Closed Volumes A, Which is Saturated with Water, and B Containing Water in an Unsaturated State

Both *A* and *B* are set at the same temperature, *T* and have the same volume,

V. Assume *A* has a quantity of water in excess of that quantity which is necessary to saturate it with water vapor. Assume *B* has water vapor in an unsaturated state. The humidity of *B* relative to *A* is defined as a percentage,

$$\mathrm{RH} = \frac{m}{m_s} 100 \tag{1.1}$$

where m is the mass of unsaturated water vapor in *B* and m_s is the mass of saturated water vapor in *A*. If we incorporate the ideal gas law equations,

$$pV = \frac{m}{\mathrm{M}_w} RT \tag{1.2}$$

and

$$p_s V = \frac{m_s}{\mathrm{M}_w} RT \tag{1.3}$$

we may alternately define relative humidity as:

$$\mathrm{RH} = \frac{p}{p_s} 100 \tag{1.4}$$

where p and p_s are the pressures of the unsaturated and saturated water vapors respectively and M_w is the molecular weight of the water. We may assume that the pressures, p and p_s are independent of the pressure exerted by any other gas in the chambers *A* and *B* provided the additional gas does not condense or react and the overall pressure in each chamber remains near atmosphere.

Capacitive relative humidity sensors were introduced in the early 1950's and remain an important tool for measuring humidity. The basic structure is shown in Figure 1-2. It consists of a bottom electrode, a dielectric whose permittivity, ϵ, varies in functional relationship to the relative humidity of its environment, and an upper electrode which is often water permeable. The first material investigated extensively as a dielectric for the capacitive sensor was aluminum oxide by Jason and others in 1952 [11], although Jason notes that a

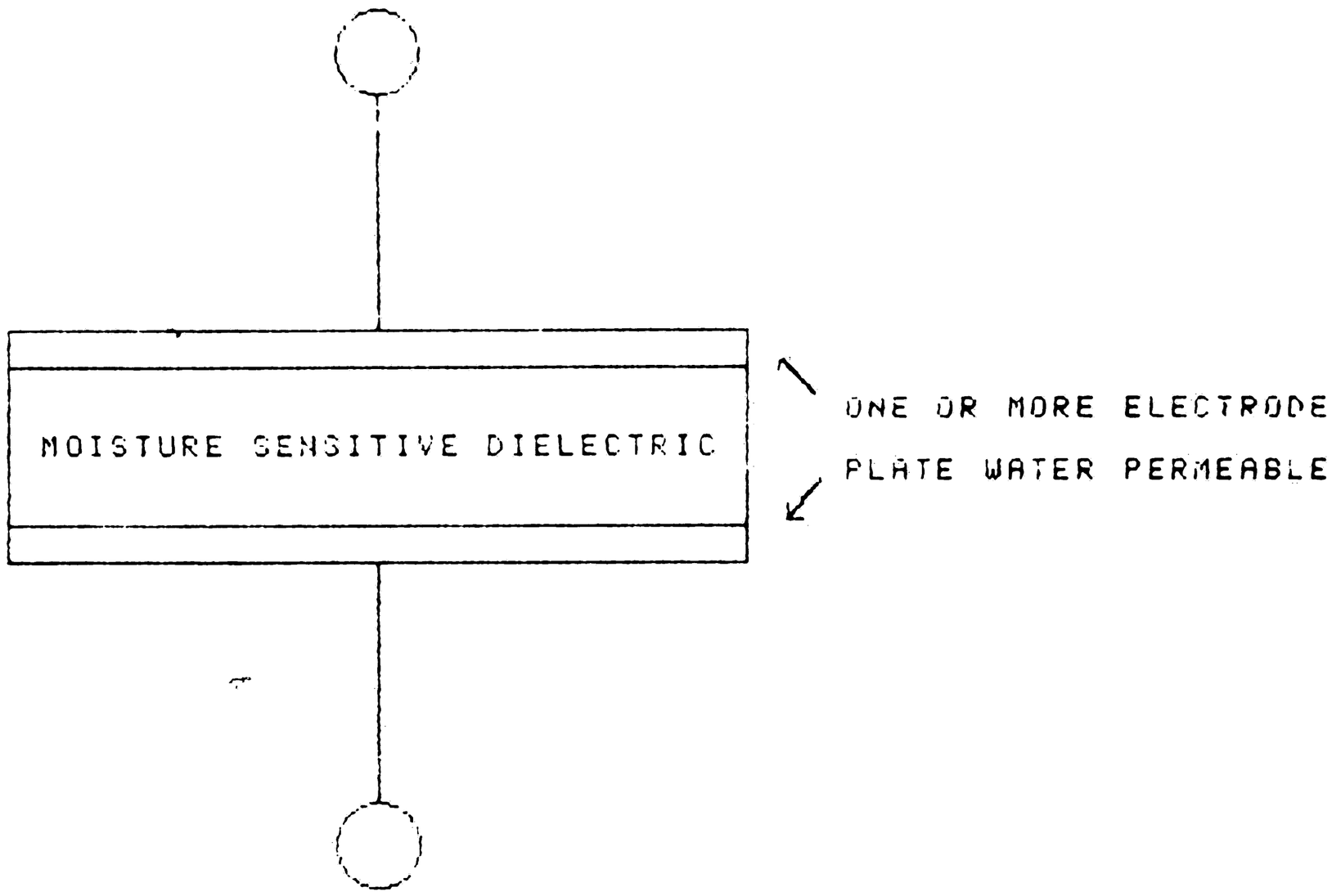


Figure 1-2: Basic Structure of a Capacitive Hygrometer

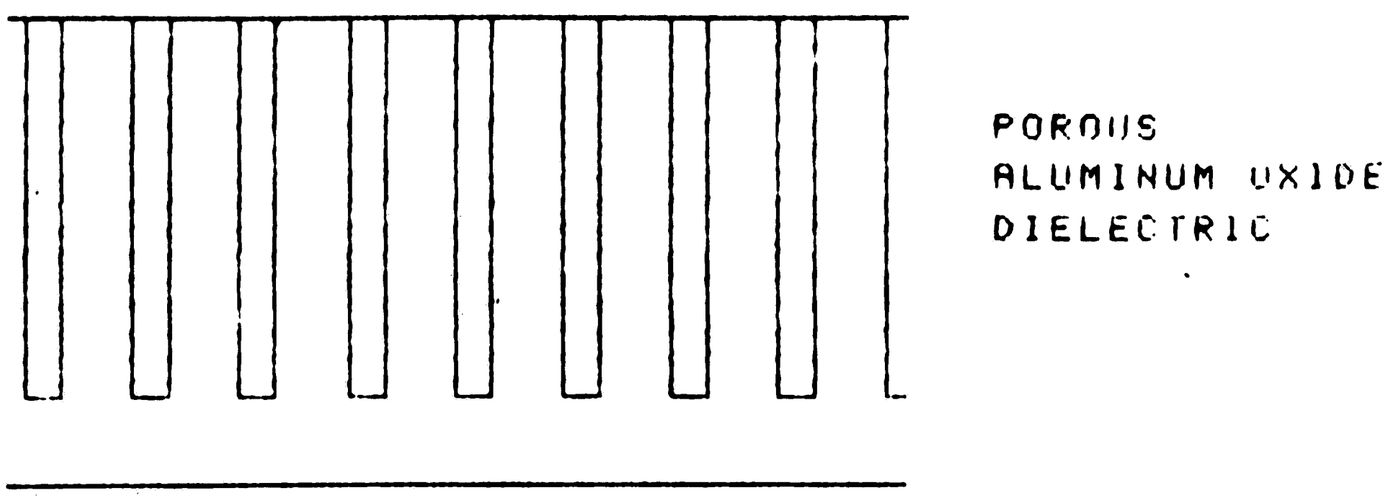
patent on an aluminum/aluminum oxide/metal hygrometer was awarded in 1941 [15]. The structure of the sensor usually consists of an aluminum plate for the bottom electrode, a porous aluminum oxide for the next layer which is formed by anodizing the bottom layer and a porous metal for the top layer. The impedence of this sensor has both a capacitive and a resistive component which vary with ambient humidity and arises from the complex structure of the porous aluminum oxide [12]. Figure 1-3 shows the structure of an aluminum oxide sensor and an equivalent circuit proposed by one author [10].

While aluminum oxide capacitive sensors suffer from poor long term stability, they have the advantages of an ability to stand up to harsh environments and have relatively fast response times. They are widely used today [10]. Aluminum oxide sensors can be manufactured with thin film and semiconductor techniques, so one could consider their incorporation into integrated sensors; however, their complex impedance response to relative humidity would require a large amount of circuitry for signal processing [2].

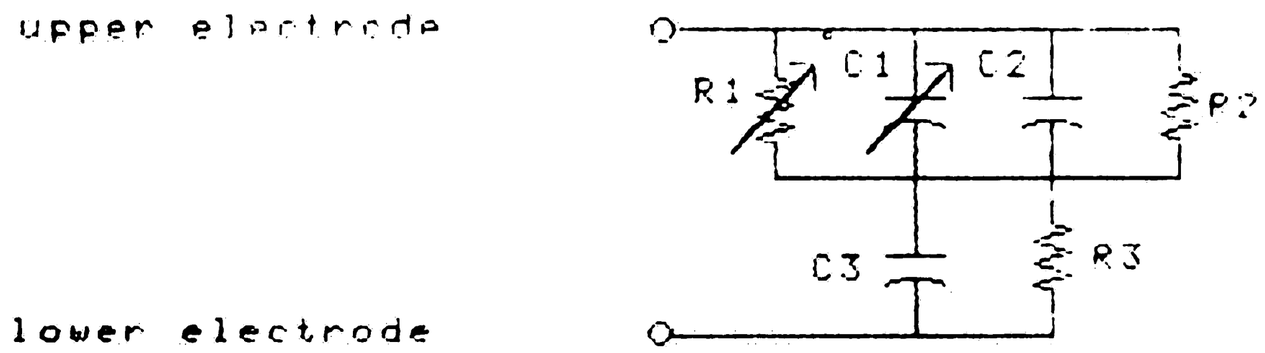
A capacitive sensor developed at Honeywell in 1965 is an example of an early use of a polymer as a dielectric whose permittivity is a function of the moisture content of its environment. David Nelson and Elias J. Amdur listed several desirable properties as a criteria for selection of a polymer for their sensor. They were:

1. Low water absorption, approximately 0.5 per cent equilibrium water absorption for 100 percent RH. This we determined would cause about a 10% change in dielectric constant which is adequate for instrumentation, but not enough to unduly lengthen the response time.

2. High water vapor permeability is necessary to insure a rapid response to a change in humidity.



(a)



R1 Moisture dependent variable resistance term
C1 Moisture dependent variable capacitance term
R2 Shunting resistance of bulk oxide between pores unaffected by moisture
C2 Shunting capacitance of bulk oxide between pores unaffected by moisture
R3 Series resistance below pores unaffected by moisture
C3 Series capacitance below pores unaffected by moisture

(b)

Figure 1-3: Aluminum Oxide Sensor (a) Structure and (b) Equivalent Circuit

3. Good strength, resilience, stiffness and resistance to creep in order that the base capacity of the sensor will be stable.

4. High resistance to chemical attack and a low permeability to contaminating.

5. High volume resistance so that the dissipation factor of the condensor will stay at a low level for all temperature-humidity conditions we wish to sense.

6. The ability to maintain these properties over a wide range of temperature and humidity [17].

We could assert that these criteria for polymer selection are still valid. The polymer Nelson and Amdur selected was Delrin. At room temperature the dielectric constant of the Delrin in the sensor varied from 3.6 to 4.1 for a sweep in humidity from 10 percent to 90 percent. Since the equivalent circuit of the sensor with a polymer dielectric may be represented by one resistor and one capacitor in parallel, the analysis of the sensor is much simpler than the aluminum oxide sensor [17].

Many discrete capacitive sensors with polymer dielectrics have since been developed. One class of polymer currently being investigated is the polyimide group. Polyimides possess many of the desired properties expressed above. They have excellent chemical resistance, and they can withstand temperatures as high as 400 degrees Centigrade in air. Some of the properties of a typical polyimide, Dupont's, PI-2555 are shown in Table 1-1 [8]. The moisture properties of polyimides are discussed in Section 2.1. An additional feature of polyimides is that when they are packaged in a liquid solvent, they can be spun on a substrate and baked to provide a uniform thin film. This thin film in turn may be rendered into small structures by photolithography; therefore, as with aluminum oxide sensors, many discrete sensors with polymer dielectrics are

Property	Typical Value
Tensile Strength	19,000 psi
Elongation	10%
Flexibility	180° Bend, No Cracks
Final Decomposition Temperature	560°C
Dissipation Factor (1KHz)	.002

Table 1-1: Some Properties of Dupont's Fully Cured Polyimide Film

manufactured using thin film and semiconductor processes.

Finally, the trend in sensor production today is toward integrated sensors. An integrated sensor is one which incorporates a sensing element fabricated usually on a semiconductor chip along with signal processing circuits. One author provides a list of integrated sensors currently under development. They are shown in Table 1-2.

Integrated Sensors Under Development

*Visible Imaging	*Temperature
*Infrared Imaging	*Moisture/Humidity
*Pressure	*Gas Composition
*Acceleration	*Ionic Concentration
*Position	*Magnetic Field
*Flow	*Potential Distribution

Table 1-2: A List of Some Integrated Sensors Under Development

Another author lists some of the possible uses for the circuitry that accompanies the sensing element in an integrated sensor as shown in Table 1-3 [14].

Possible Functions of the Circuitry in Integrated Sensors
*Output Impedance Transformation
*Amplification
*Temperature Compensation
*Power Supply Variation Compensation
*Offset Balance
*Filtering of Unwanted Signals
*Corrections for Nonlinearity of Sensor Output
*A/D Conversion
*Multiple Sensor Output Averaging
*Sensor Operation Checks and Alarms
*Conversion of the Sensor Output for
*Telemetry
*Pattern Recognition
*Power Reduction
*Processing of Signals from Several Different Sensors Sensing Different Physical Quantities

Table 1-3: Circuit Functions in Integrated Sensors

As the list shows, integrated sensors are being put to many uses.

1.2 Purpose of the Work

This thesis reports on the synthesis of an integrated relative humidity sensor using some heretofore separate technologies of manufacturing discrete capacitive sensors and integrated circuits. Using resources available at Leeds and Northrup Co. and at Lehigh University, a development team at L&N designed and manufactured some sensors. This paper presents the following.

1. The first subject is the response of polyimides to ambient relative humidity, RH. Specifically this work considers the humidity response of the polyimide's permittivity, ϵ. The funcional relationships between ϵ and RH derived in two separate studies are considered. The incorporation of a moisture sensitive polymer as a dielectric in a discrete capacitive humidity sensor is discussed.

2. The second subject is a circuit designed to measure the capcitance of a relative humidity sensing element and provide a D.C. voltage level output. The thesis describes the circuit's operation and the effect of circuit parameters on the linear relationship the output has with measured capacitance.

3. The third subject is the design of structures for the sensing element and two reference capacitors required by the measuring circuit. The paper considers two alternatives for reference capacitor design.

4. The fourth subject is the process of manufacturing the sensor. The thesis describes process design and photomask layout considerations. Difficulties encountered in actual fabrication are described.

5. The final subject is the preliminary testing of some functioning sensors. The paper presents some results along with some recommendations and conclusions.

Chapter 2
Theory of Circuit Operation

2.1 Sensor Theory

The phenomenon that is the basis of this capacitive relative humidity sensor is the variation of the permittivity, ϵ, of a thin polyimide film with the relative humidity of the environment to which it is exposed. If one constructs a capacitor, such as the one shown in Figure 2-1, the capacitance, given by $C=\epsilon\frac{A}{t}$, where ϵ would be a function of the relative humidity where A is the effective area of the plates and t is the thickness of the polyimide film. Several features are desirable about the functional relationship between permittivity and relative humidity, $\epsilon=f(\mathrm{RH})$, of the dielectric used in a capacitive humidity sensor.

- It is desirable that the function be linear. If the relationship is not, one must use external circuitry to linearize the final output of the sensor. A target would be a linearity of $\pm 1\%$.

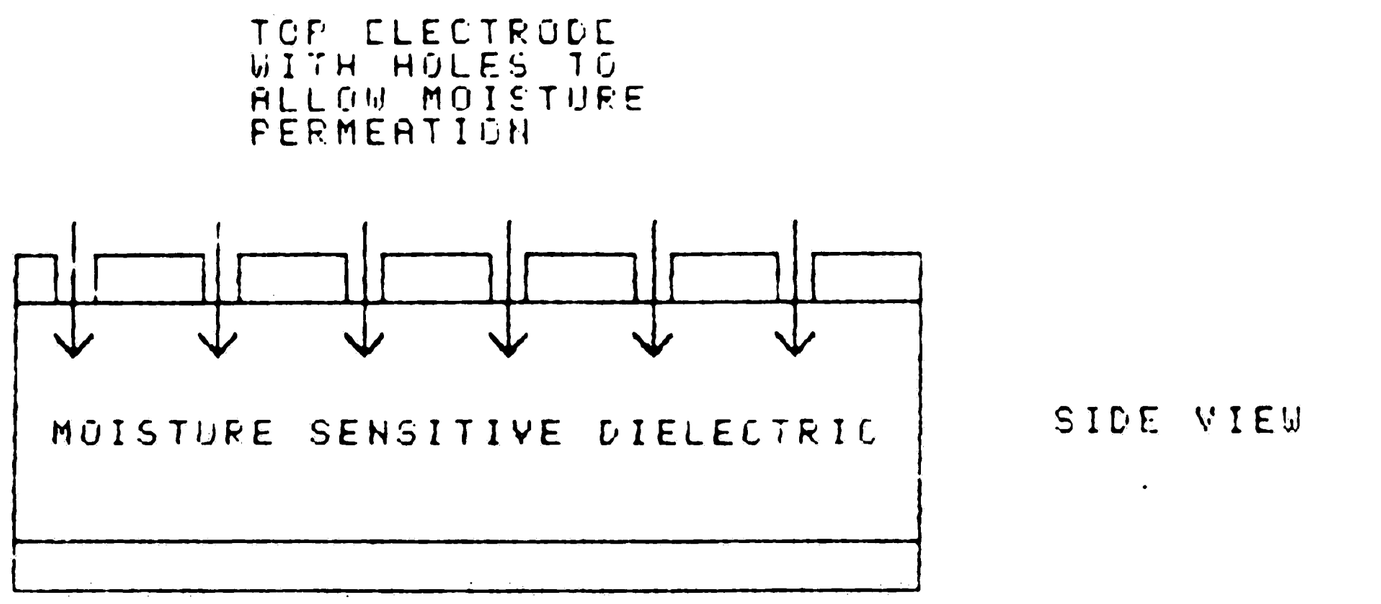
- It is desirable that hystereis be small. In other words the functional relationship, f, should yield the same values for given humidities for situations where the humidity is increased as when humidity is decreased. A target here would be $\pm 2\%$.

- It is desirable that the functional relationship be repeatable. Every time that the dielectric is exposed to a given relative humidity it should yield the same value of f. A target would be $\pm 1\%$ RH.

- Temperature dependence should be minimal.

- The response time of the dielectric to changes of the relative humidity in its environment should be small. A target would be 30 seconds.

Authors have evaluated the moisture properties of polyimides not so much with the object of creating sensors, but with the object of determining the value



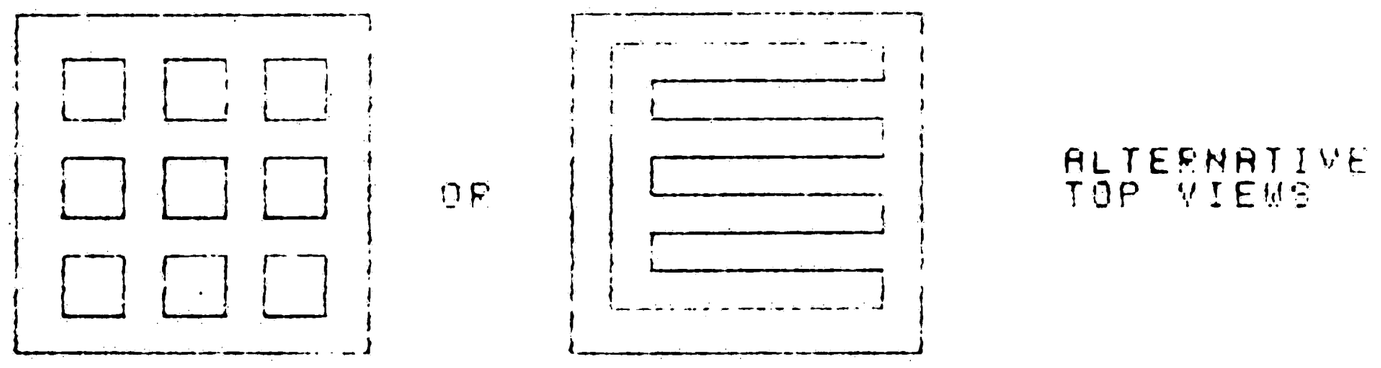


Figure 2-1: Basic Humidity Sensitive Capacitor

of polyimides as intermetal layer and passivating dielectrics. Wilson evaluates several types of polyimides for their moisture barrier properties and considers the effects of various cure processes on moisture permeation [21]. He concludes that if the polyimide has been properly applied and cured, it provides as good a moisture barrier as any other known semiconductor passivant.

Samuelson and Lytle investigated the polorization effects due to absorbed water in polyimides. They performed C-V (capacitance versus voltage) analyses on MIS (Metal Insulator Semiconductor) structures consisting of silicon substrates, thermal oxide, silicon nitride, Hitachi's PIQ-13 polyimide and a metallization of aluminum-copper -silicide. As a result of their measurements, they identify three types of absorbed water, free water, unassociated molecular water, and H bonded water to describe the polarization effects that they observe [18].

Schubert and Nevin made a capacitive humidity sensor roughly equivalent to that shown in Figure 2-1 [19]. Having measured the response of their sensor, they reviewed the literature to determine the theoretical basis of its operation [20, 13, 1]. To describe the behaviour of the polyimide dielectric as it absorbs water, they chose Looyenga's equation for the dielectrid constant, ϵ[1] of mixture:

$$\epsilon=(v_2(\epsilon_2^{\frac{1}{3}}-\epsilon_1^{\frac{1}{3}})+\epsilon_1^{\frac{1}{3}})^3 \tag{2.1}$$

where ϵ_1 and ϵ_2 are the dielectric constants of the polymer and water, respectively, and v_2 is the fractional volume of water absorbed. To determine v_2, they use an equation derived by Dubinin [7] to describe the absorption of a gas into a solid. Dubinin's equation is:

---

[1]There seems to be some confusion in the literature in that ϵ sometimes represents permittivity and at other times represents the dielectric constant.

$$v = v_m^o \exp(-(RT \ln x/E)^n - \alpha(T - T_o)) \tag{2.2}$$

where v_m^o is the maximum fractional volume of absorption at temperature, T_o, R is the universal gas constant, T is the absolute temperature, α is the thermal coefficient of limiting absorption, n is an empirical factor and E is the free energy of absorption.

Using equations (2.1) and (2.2), Schubert and Nevin derived the following expression for the capacitance of their sensor:

$$C = (0.287X^{1.725} + 3.553)^3 \tag{2.3}$$

where X is percent relative humidity divided by 100. Using a value of 2.93 for the dielectric constant of polyimide and 80.0 for the dielectric constant of water, they claim excellent agreement with experimental data.

Schubert and Nevin measured two characteristics of their sensor, response time and long term stability. They find their typical response times to be around 30 seconds. The results of their long term stability tests indicate a drift of 0.34 percent in capacitance which would cause an error of 4 percent in the sensor's zero reading of relative humidity. On the basis of this data, they draw an interesting conclusion.

> Thus this type of a sensor would benefit from a differential technique for readout such that a second sensor structure, not exposed to humidity would be used on the same die [19].

The idea of the use of a second sealed sensor structure is in fact one of the approaches used in the design of our integrated sensor.

Perhaps the most exhaustive and thorough study of the relationship of a polyimide's permittivity with ambient relative humidity has been undertaken by Senturia and others with work done separately at MIT as well as with work

done jointly at MIT and IBM [5, 6, 4]. Using various structures similar to Figure 2-1, the authors performed a number of different experiments.

One experiment was to measure the change in weight of a capacitor structure as a function of ambient relative humidity. Denton and others found the linear relationship expressed by the following equation.

$$\frac{m}{m_D} = 1 + .00021(\mathrm{RH}) \tag{2.4}$$

where m is the mass of the polyimide dependent on relative humidity, m_D is the mass of the polyimide at 0 percent relative humidity and RH is the relative humidity in percent [5].

In another experiment, Senturia and others measured the relationship of the capacitance of their structure and the ambient relative humidity and derived the following expression for the dielectric constant, ϵ(RH):

$$\epsilon(\mathrm{RH}) = 3.37 + 0.01(\mathrm{RH}) \tag{2.5}$$

where RH is the percent relative humidity [6]. As mentioned above, the linear relationship found in (2.5) makes the polyimide a desirable dielectric film for incorporation in a sensor.

Using equations (2.4) and (2.5) and some additional considerations, the authors calculated the number of dipoles per unit volume and the number of water molecules per unit volume in polyimide as a function of relative humidity. These calculations allowed them to determine the polarization of absorbed water molecules in polyimide. They conclude that for the most part the absorbed water has a dipole moment nearly equal to that of free water [6]. They find the polyimide moisture to be reversible, which is an important consideration when designing a capacitive sensor with low hysteresis.

In other work, Senturia and others subjected their capacitor structures to swings in relative humidity and measured the capacitance versus time response. From this response they extracted a room temperature diffusion constant of moisture through polyimide of 5×10^{-9} cm.^{2}/sec . Observing the diffusion constant response to temperature, they extracted an activation energy of .32 eV.. The diffusion constant is important in that the response time of a polyimide based capacitive humidity sensor will depend on this constant and the length of the diffusion path [4].

Finally, consider an example of a commercially available capacitive humidity sensor, manufactured by HyCal Engineering in El Monte, California. Its structure, shown in Figure 2-2, consists of an alumina substrate, two sets of interdigitated thin film metal electrodes, a thermosetting polymer layer which is water absorbing, an isolated water permeable conductive mesh, and a second water absorbing film. The capacitor is actually two capacitors in series: one being from one set of metal fingers through the lower polymer to the mesh, and the other consisting of the mesh, the lower polymer layer and the other set of fingers. Sensor operation occurs when water diffuses through the upper polymer layer, through the permeable mesh, and equilibrates with the lower polymer dielectric.

The effective sensor response time is governed by the thickness of the two polymer layers. The capacitance of the device is given by the equation:

$$C=\frac{Nlw\epsilon}{2t_1} \tag{2.6}$$

where l is the finger length, w is the finger width, N is the number of fingers, ϵ is the permittivity and t_1 is the thickness of the lower polymer.

Table 2-1 shows some of the operating characteristics of the sensor.

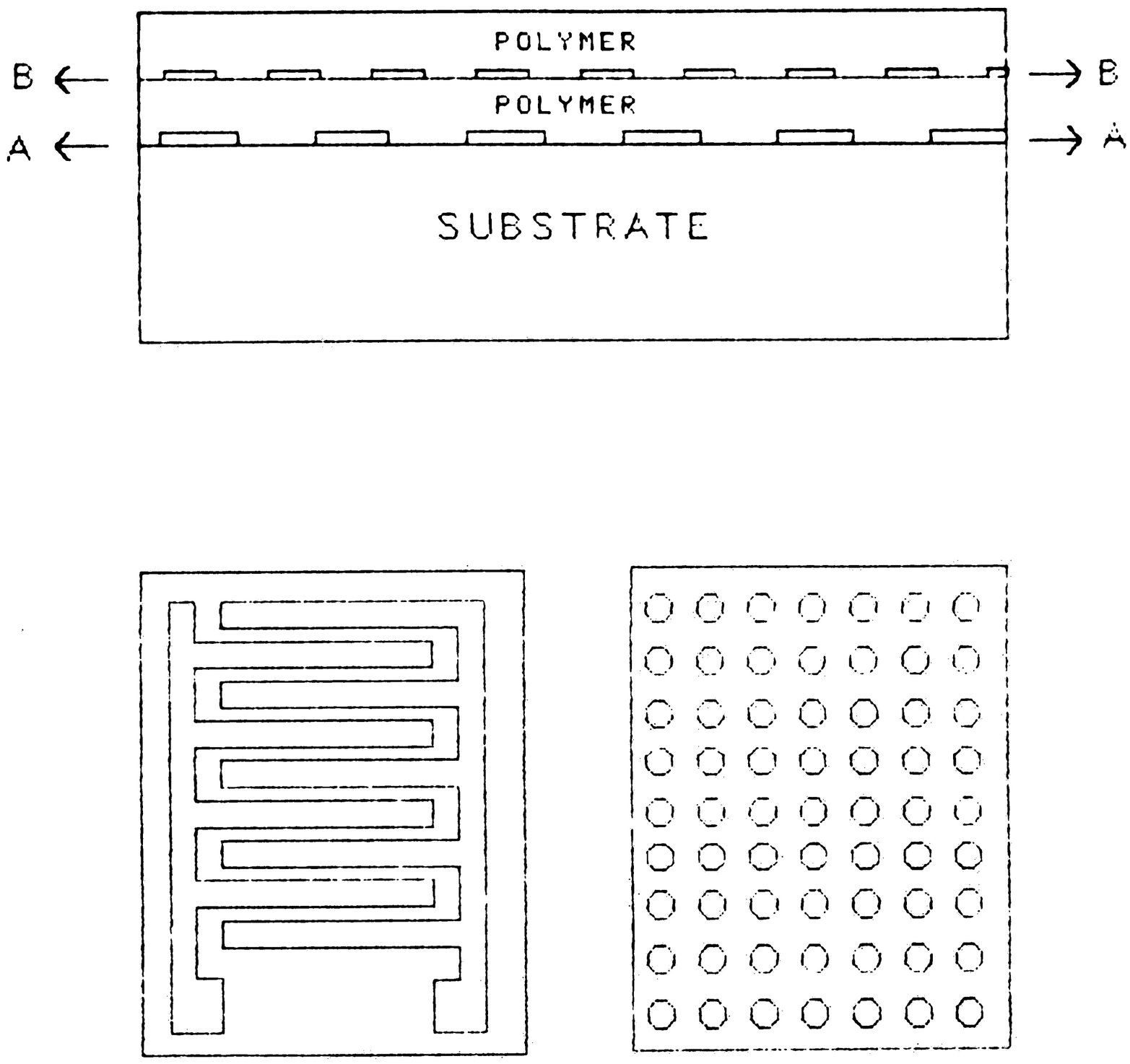


Figure 2-2: Structure of the HyCal Humidity Sensor

Operating Characteristics of HyCal's Capacitive Humidity Sensor

Performance Characteristic	Tested Value
Capacitance at 11.3% RH, pf.	72-92
Output Range 11.3 to 93.8% RH	27
Hysteresis Span, % RH	1.5
Deviation from, Linearity	-6.5
16 Hour Drift at 93.8% RH, in % RH	3
Time Constant, Sec.s	20
Temperature Coefficient (% RH/°C)	$-.05\,RH - .0035\frac{RH}{T}$

Table 2-1: Operating Characteristics of HyCal's Capacitive Humidity Sensor

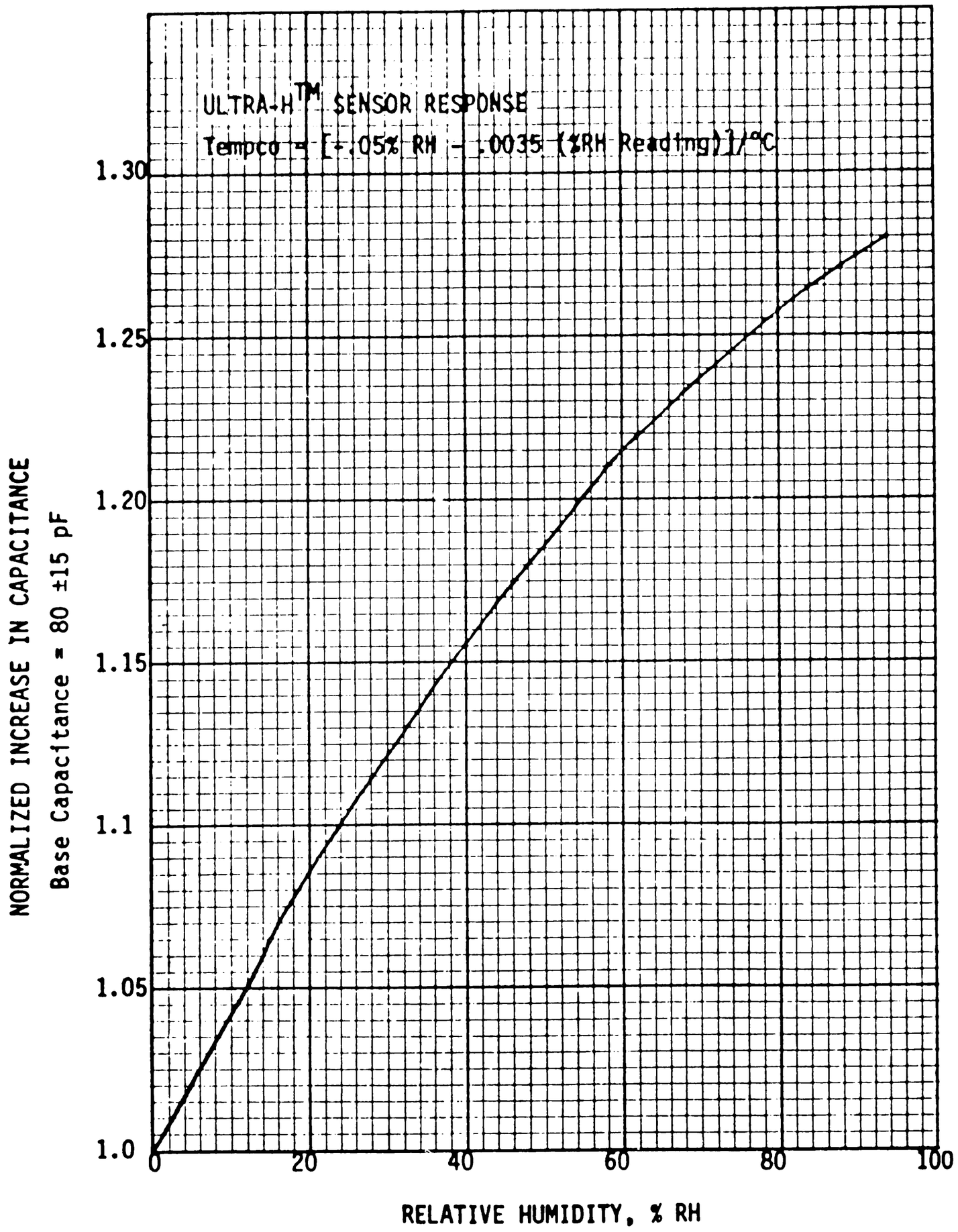


Figure 2-3: Normalized Humidity Response of HyCal Humidity Sensor

Figure 2-3 shows the normalized sensor response to humidity. As can be seen in the next chapter, the sensing element of our integrated sensor incorporates a conductive mesh similar to the HyCal sensor as its top plate [3].

2.2 Measuring Circuit Theory

The measuring circuit's purpose is to take as an input the capacitance of the humidity sensing capacitor and to provide as an output a voltage proportional to the input. The entire circuit is shown in Figure 2-4. It consists of four sections. Three of the sections, Charge Balance, Comparator and Integrator comprise the three stages of the capacitance measuring circuit. The fourth section is a circuit to provide a two phase non-overlapping clock signal to operate switches.

Figure 2-5 shows the output of the clock circuit. The circuit uses conventional digital CMOS technology. (See Appendix A for the details of the design of the clock circuit.) The non-overlapping clocks are used to provide smooth action for the switched capacitors of the circuit allowing them to go from charging up at one voltage to discharging at another as shown in Figure 2-6.

The Charge Balance circuit consists of the sensing capacitor, called C_x and two reference capacitors, C_o and C_{ref} . One side of each of the capacitors is tied to node 1 of the circuit as shown in Figure 2-4. The other side of the capacitors is connected to various voltage sources by the switching transistors during the two phases of operation.

Figure 2-7(a) shows the condition of the Charge Balance stage of the circuit during the first or set up phase of circuit operation. (Φ_1 is high.) V_{ref} is nothing more than the positive power supply voltage of the circuit. V_{t1} is the threshold or trigger of the succeeding Comparator Stage. V_{t1} is produced by

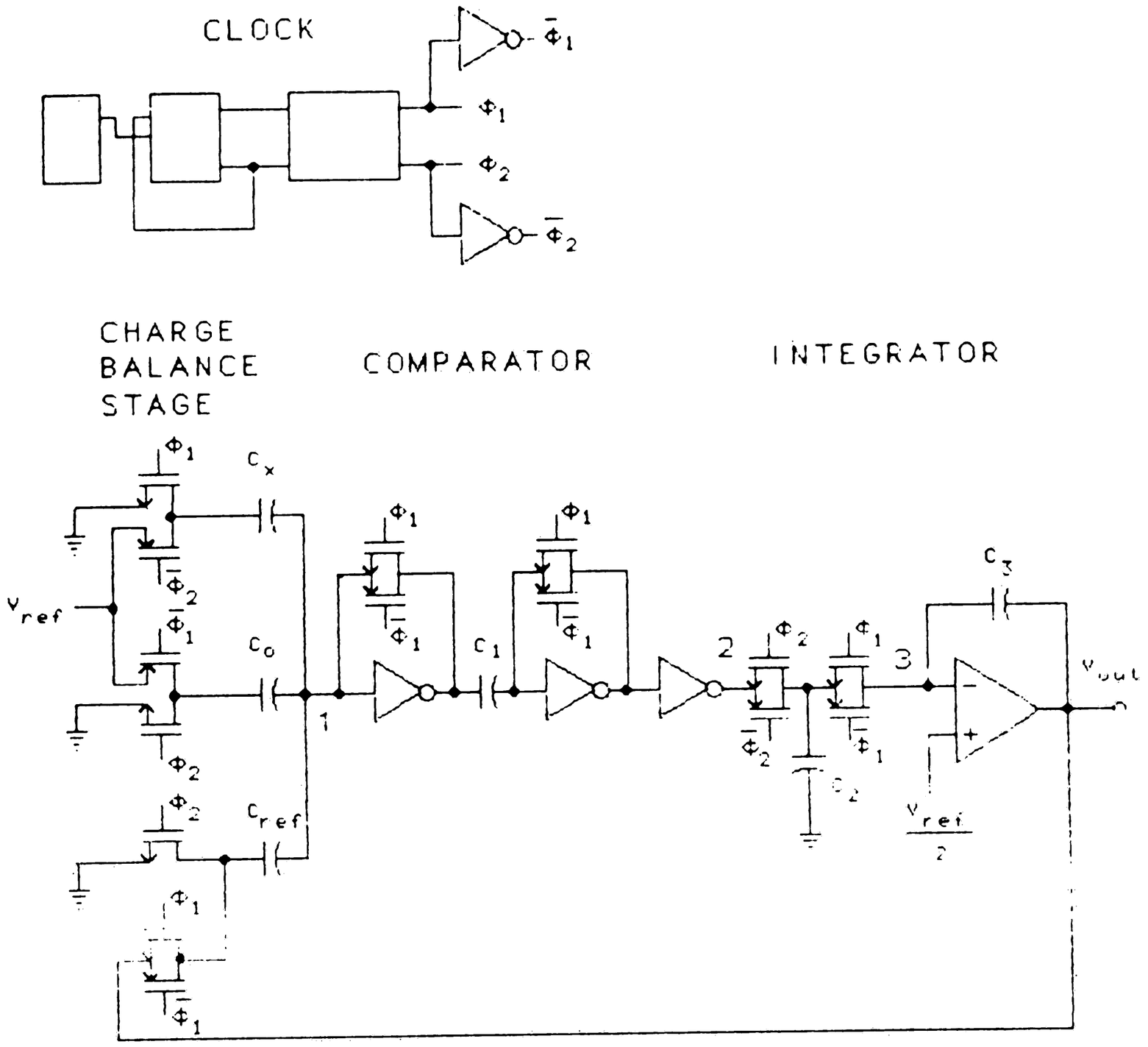


Figure 2-4: Capacitance Measuring Circuit for the Integrated Relative Humidity Sensor

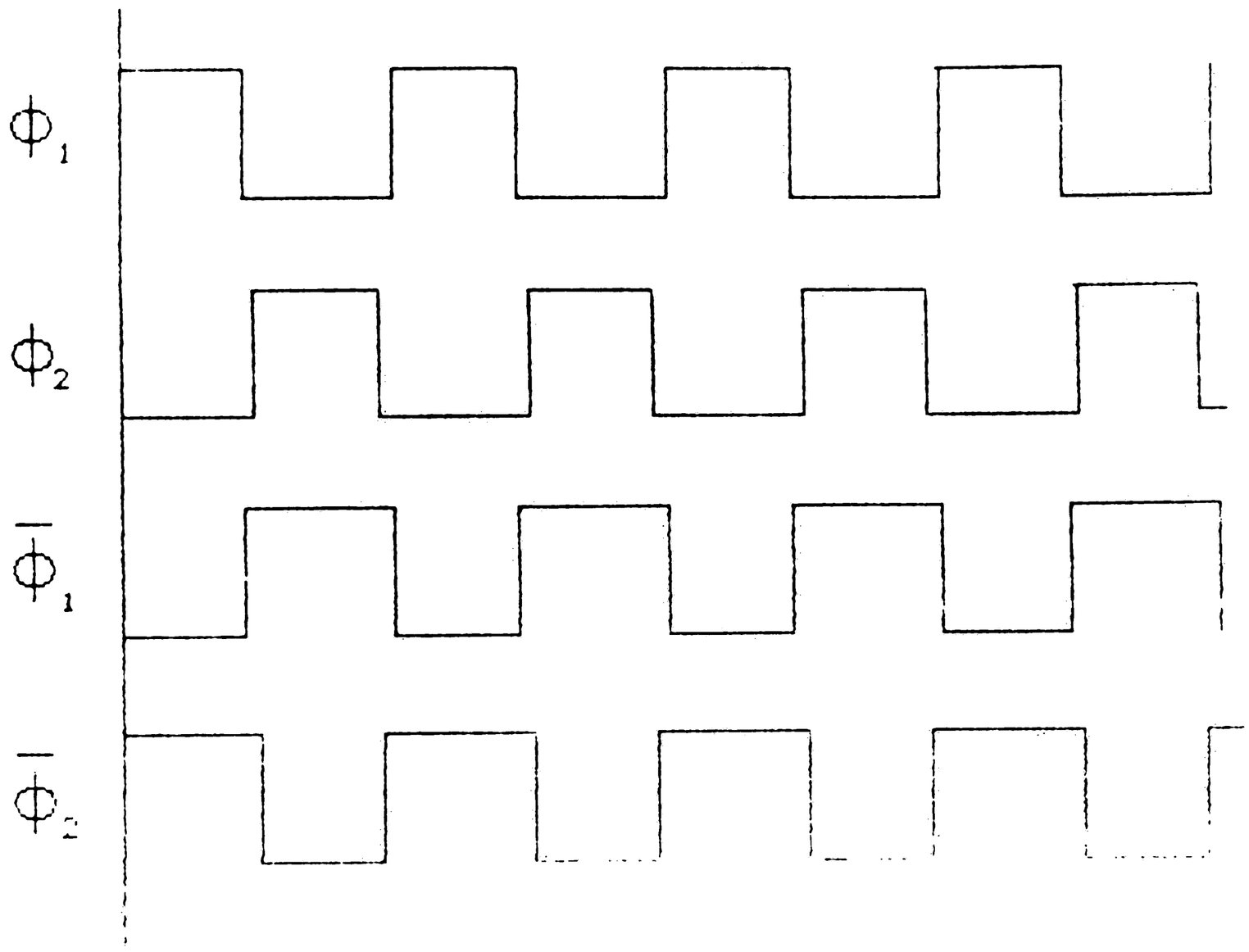


Figure 2-5: Two Phase Non-Overlapping Clock Signal

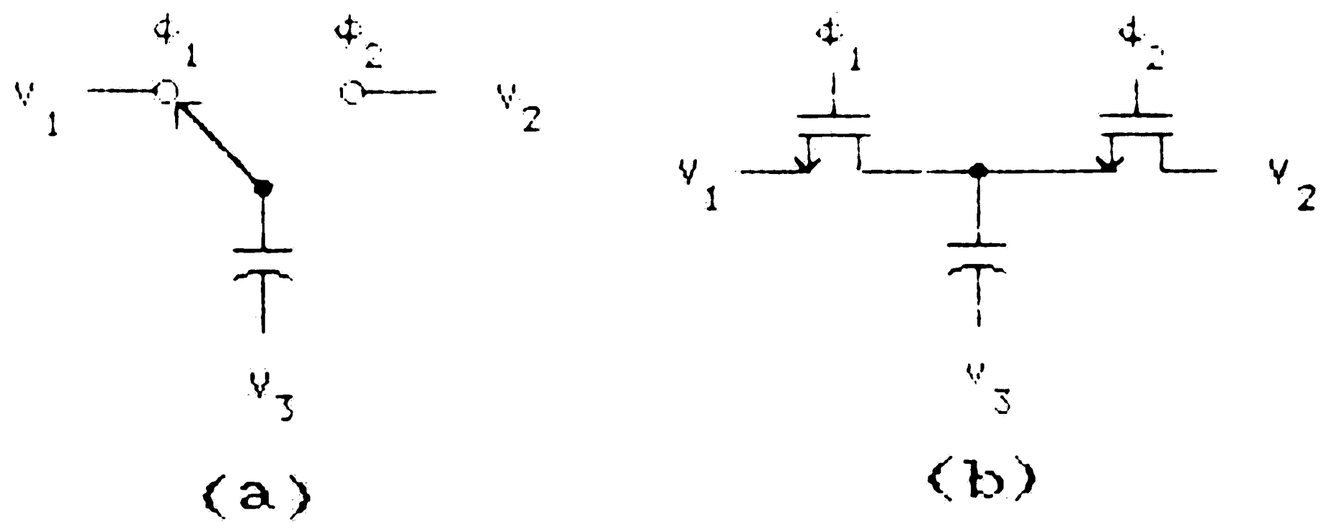


Figure 2-6: Switched Capacitor, (a) Conceptual, (b) Two Transistor Implementation, (c) Transmission Gate Implementation

the input invertor of the Comparator stage during phase one as shown below. V_{out} is the output voltage of the entire circuit being fed back at this stage. If Q_{Cx1}, Q_{Co1} and Q_{Cref1} are the charges on C_x, C_o and C_{ref} respectively during this first phase then:

$$Q_{Cx1}=C_x(-V_{t1}) \tag{2.7}$$

$$Q_{Co1}=C_o(V_{ref}-V_{t1}) \tag{2.8}$$

and

$$Q_{Cref}=C_{ref}(V_{out}-V_{t1}) \tag{2.9}$$

The total charge on all three capacitors during this phase, Q_{tot1}, is given by:

$$Q_{tot1}=C_x(-V_{t1})+C_o(V_{ref}-V_{t1})+C_{ref}(V_{out}-V_{t1}) \tag{2.10}$$

Figure 2-7(b) shows the condition of the Charge Balance Stage during the measuring phase of circuit operation. (Φ_2 is high.) During this phase, node 1 of the circuit is no longer connected to any voltage supply and is allowed to assume a new voltage, V_{sum}. The charges on C_x, C_o and C_{ref} become during phase 2:

$$Q_{Cx2}=C_x(V_{ref}-V_{sum}) \tag{2.11}$$

$$Q_{Co2}=C_o(-V_{sum}) \tag{2.12}$$

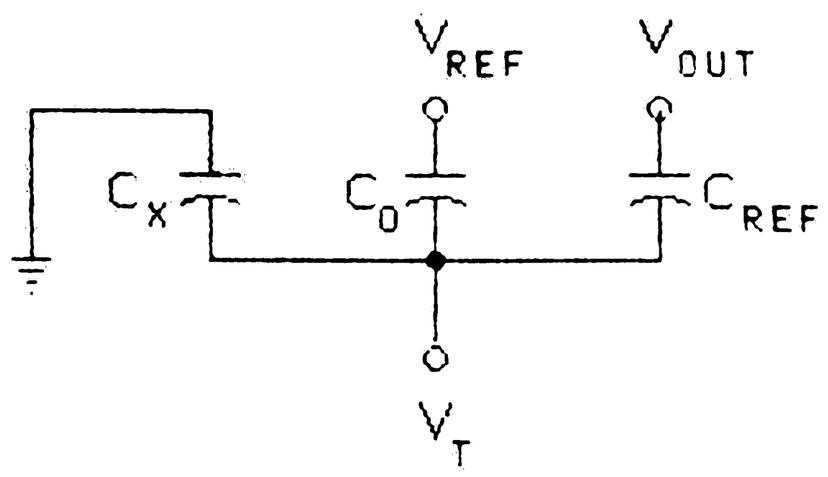
and

$$Q_{Cref2}=C_{ref}(-V_{sum}) \tag{2.13}$$

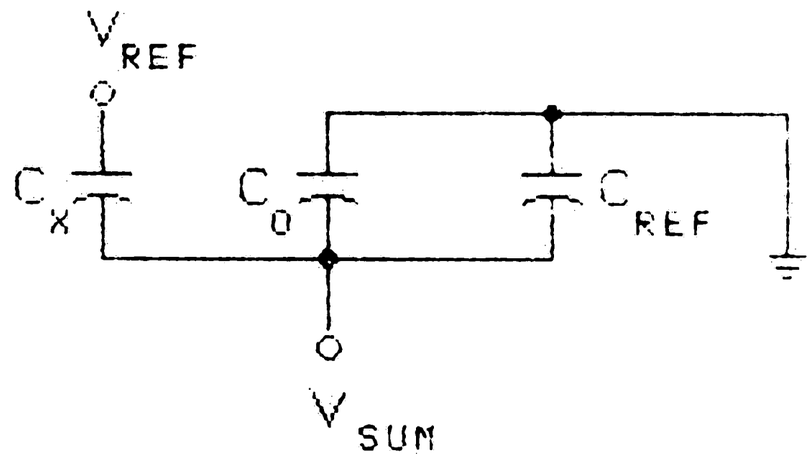
The total charge, Q_{tot2} becomes:

$$Q_{tot2}=C_x(V_{ref}-V_{sum})-C_oV_{sum}-C_{ref}V_{sum} \tag{2.14}$$

During the transistion from Phase One, the set up part of circuit operation, to Phase Two, the measuring part, node 1 changes from being set at V_{t1}, by the succeeding comparator stage to becoming an input gate; therefore, while



(a)



(b)

Figure 2-7: Condition of the Charge Balance Stage During (a) Phase 1, and (b) Phase 2

node 1's voltage is changing to V_{sum}, no charge can flow out of pin 1 and the total charge on all three capacitors is conserved. From equations (2.10) and (2.14) one obtains:

$$Q_{tot1}=Q_{tot2} \tag{2.15}$$

or

$$\begin{aligned} &C_x(-V_{t1})+C_o(V_{ref}-V_{t1})+C_{ref}(V_{out}-V_{t1})= \\ &C_x(V_{ref}-V_{sum})+C_o(-V_{sum})+C_{ref}(-V_{sum}) \end{aligned} \tag{2.16}$$

or

$$V_{sum}=V_{t1}+\frac{C_x-C_o}{C_x+C_o+C_{ref}}V_{ref}-\frac{C_{ref}}{C_x+C_o+C_{ref}}V_{out} \tag{2.17}$$

The function of the two succeeding stages of the circuit is to adjust the output voltage, V_{out}, so that V_{sum} becomes V_{t1}. From equation (2.17) one can see that when this occurs:

$$V_{out}=\frac{C_x-C_o}{C_{ref}}V_{ref} \tag{2.18}$$

the output voltage, V_{out} is proportional to C_x with an offset of $\frac{C_o}{C_{ref}}V_{ref}$; therefore, one can control the linear relationship of V_{out} to C_x by selection of C_o and C_{ref}

Figure 2-8 shows the Comparator Stage of the circuit. It consists of two switched inverters, X_1 and X_2 coupled by capacitor C_1 and a buffer stage, X_3. During the first phase of circuit operation, the input and outputs of each of the switched inverters are shorted together. This causes each inverter to balance at their respective threshold voltages, V_{t1} and V_{t2}. At the same time V_{t1} is applied to node 1 of the Charge Balance stage. During the second phase, the switches shorting the invertors open and node 1, the input of the Comparator Stage changes to the voltage, V_{sum}. If $V_{sum} > V_{t1}$, then the output of the com-

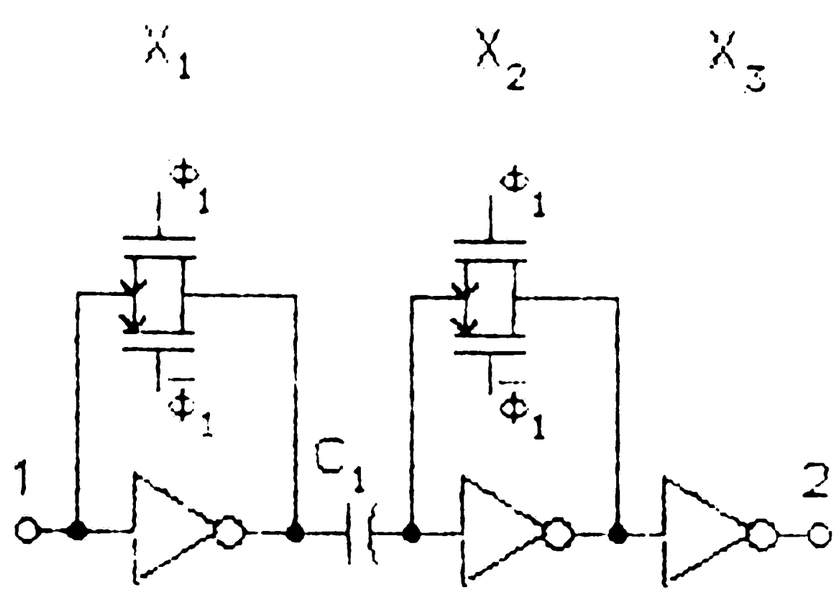


Figure 2-8: Comparator Stage

parator stage at node 2 of the circuit goes low. If $V_{sum} < V_{t1}$, the output voltage goes high at node 2. The coupling capacitor, C_1, stores any differences between X_1's threshold voltage, V_{t1} , and X_2's threshold voltage, V_{t2}, but couples the output of X_1 to the input of X_2. Cascading X_1 and X_2 and adding the buffer stage increase the gain of the Comparator stage.

The Integrator Stage, shown in Figure 2-9, also has two phase operation. The operation of this stage is best understood when we begins by considering the second phase condition of the stage first. During Phase 2, (Φ_2 high), the capacitor, C_2, is connected to node 2 and "reads" the output of the comparator

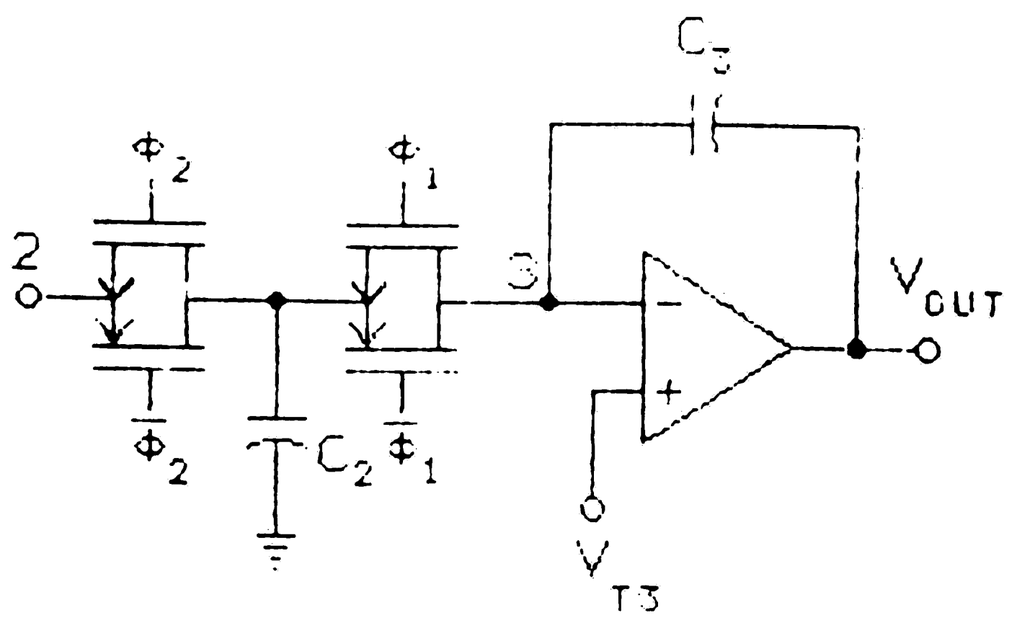


Figure 2-9: Integrator Stage

stage; that is, C_2 is charged up by whatever voltage is on node 2. During the subsequent phase, C_2 is connected to the inverting input of the op amp and transfers its charge. If $V_{2\Phi 2}$ is the voltage on node 2, $V_{3\Phi 2}$ the voltage on node 3 and $V_{out\Phi 2}$ is the output voltage during Phase 2, then the charge, $Q_{2\Phi 2}$, on C_2 and the charge $Q_{3\Phi 2}$ on C_3 can be given by the equations:

$$Q_{2\Phi 2}=C_2V_{2\Phi 2} \tag{2.19}$$

and

$$Q_{3\Phi 2}=C_3(V_{out\Phi 2}-V_{3\Phi 2}) \tag{2.20}$$

After charge has been transferred from C_2 to the integrator during Phase 1, the charge, $Q_{2\Phi 1}$ on C_2 and $Q_{3\Phi 1}$ on C_3 can be given by the equations:

$$Q_{2\Phi 1}=C_2V_{3\Phi 1} \tag{2.21}$$

and

$$Q_{3\Phi 1}=C_3(V_{out\Phi 1}-V_{3\Phi 1}) \tag{2.22}$$

where $V_{3\Phi 1}$ and $V_{out\Phi 1}$ are the voltages at node 3 and the output respectively during the subsequent Phase 1. When charge transfers during Phase 1, the current in C_2 can be equated to the current in C_3.

$$\frac{\Delta Q_2}{\Delta t}=\frac{\Delta Q_3}{\Delta t} \tag{2.23}$$

so

$$Q_{2\Phi 1}-Q_{2\Phi 2}=Q_{3\Phi 1}-Q_{3\Phi 2} \tag{2.24}$$

and

$$C_2(V_{3\Phi 1}-V_{2\Phi 2})=C_3(V_{out\Phi 1}-V_{2\Phi 1}-V_{out\Phi 2}+V_{3\Phi 2}) \tag{2.25}$$

The voltage supplied to the non-inverting input of the op amp is generated by a shorted inverter similar to the generated trigger voltages of the comparator stages X_1 and X_2. It is designed to have a value close to $\frac{V_{ref}}{2}$. I will call it, V_{t3}. If A is the open loop gain of the op amp then the following equations can be written:

$$V_{3\Phi 1}=V_{t3}-\frac{V_{out\Phi 1}}{A} \tag{2.26}$$

and

$$V_{3\Phi 2}=V_{t3}-\frac{V_{out\Phi 2}}{A} \tag{2.27}$$

Combining equations (2.25), (2.26) and (2.27) we get:

$$V_{out\Phi 1}=\frac{C_2}{C_3}(V_{t3}-\frac{V_{out\Phi 1}}{A}-V_{2\Phi 2})+V_{out\Phi 2}+V_{t3}-\frac{V_{out\Phi 1}}{A}-V_{t3}+\frac{V_{out\Phi 2}}{A} \quad . \tag{2.28}$$

Assuming a large open loop gain, A, we can write:

$$V_{out\Phi 1}=\frac{C_2}{C_3}(V_{t3}-V_{2\Phi 2})+V_{out\Phi 2} \tag{2.29}$$

So the output voltage will change during Phase 1 of circuit operation by an amount $\frac{C_2}{C_3}(V_{t3}-V_{2\Phi 2})$ as determined by the value of the voltage on node 2 during the previous Phase 2 or measuring phase.

If $V_{t3}=\frac{V_{ref}}{2}$ and $\Delta V_{out}=V_{out\Phi 1}-V_{out\Phi 2}$ then:

$$\Delta V_{out}=\frac{C_2 V_{ref}}{C_3\ 2} \quad \text{when} \quad V_{2\Phi 2}=0$$

$$\Delta V_{out}=-\frac{C_2 V_{ref}}{C_3\ 2} \quad \text{when} \quad V_{2\Phi 2}=V_{ref}$$

The circuit resolution is determined by ΔV_{out} . Table 2-2 summarizes the overall circuit function.

This circuit design has some requirements for the physical layout. The structures of the capacitors C_x , C_o and C_{ref} must be designed so that C_o and C_{ref} do not vary with moisture. Steps must be taken during the layout to minimize stray capacitance. Each section of the circuit was simulated on SPICE, a circuit simulation program. "

Summary of Circuit Operation

Condition at Node1 During Phase 2	Output of Comparator at Node 2 During Phase 2	Integrator Adjustment of Output During Subsequent Phase1
$V_{sum} > V_{t1}$	Low	Increase by $\frac{C_2}{2C_3}V_{ref}$
$V_{sum} < V_{t1}$	High	Decrease by $\frac{C_2}{2C_3}V_{ref}$
$V_{sum} \approx V_{t1}$	Neither Fully	Steps about $\frac{C_x - C_o}{C_{ref}}V_{ref}$
Balance	High or Low	

Table 2-2: Summary of Circuit Operation

Chapter 3
Design and Fabrication

3.1 Sensor Structure

Figure 3-1 shows the conceptual sensor structure we used in this device. It consists of four layers:

1. The bottom layer is a P^+ region diffused into the N-type silicon substrate.

2. The second layer is the polyimide layer that comprises the dielectric.

3. The top electrode is a conductive mesh which allows moisture to penetrate into the polyimide dielectric in a manner similar to that of the sensor described at the end of Section 2.1

4. Another water permeable polyimide layer is formed as a top layer to protect the underlying structure from scratching and harsh environments.

This structure meets the requirement that one can manufacture the sensor using thin film and semiconductor techniques.

3.2 Reference Capacitor Structure

To meet the requirement of the circuit design that one provide reference capacitors, C_o and C_{ref} , whose capitances do not vary with ambient relative humidity, we tried two approaches.

The first approach was to use the structure shown conceptually in Figure 3-2. This structure resembles the structure shown in Figure 3-1 except that the top electrode is now a thick metal plate that serves as a barrier to moisture permeation into the lower polyimide layer. Conceivably, if the top metal plate is deposited in a vacuum system, the polyimide capacitor dielectric will be dried out and sealed in this dry state; therefore, this structure should have the same

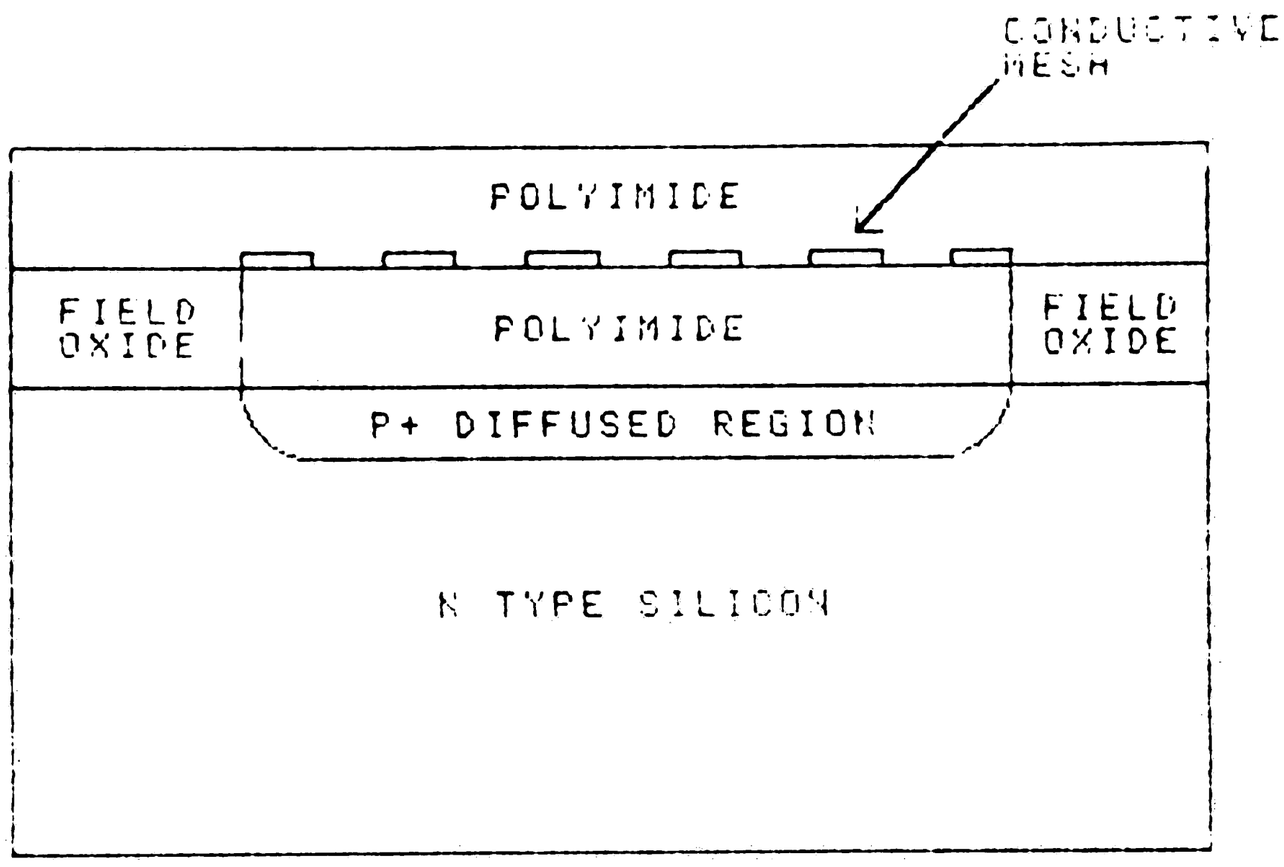


Figure 3-1: Sensing Element Structure

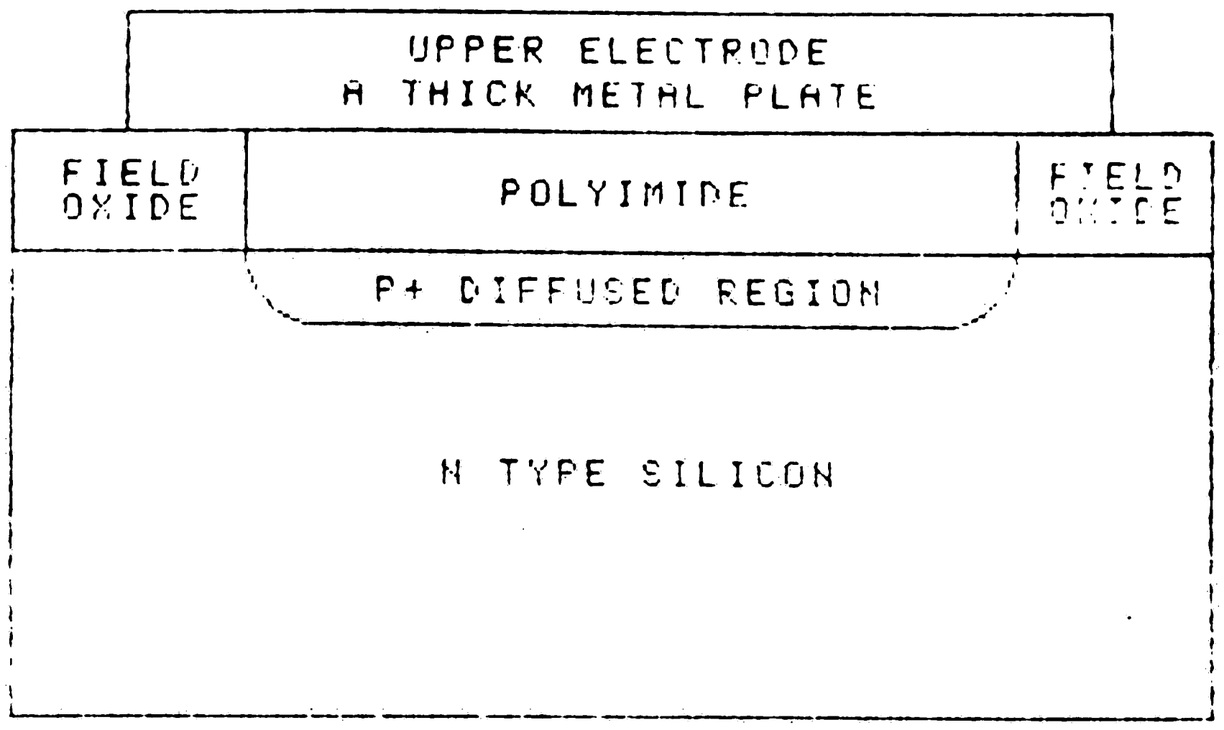


Figure 3-2: Reference Capacitor with Polyimide Dielectric

physical properties as that of the sensing structure save that of variation of permittivity of the polyimide with ambient relative humidity.

The other approach is to use the structure shown conceptually in Figure 3-3. This is a conventional capacitor structure available in CMOS technology. It consists of a lower P^+ diffused region in an N-type silicon substrate, a thermal oxide layer grown from the silicon as a dielectric and an upper metal electrode plate. Presumably this structure will not be affected by ambient relative humidity.

Both of these structures have been fabricated separately in our facility at Leeds and Northrup and tested in various humidity conditions over long periods of time for evaluation of their stability. Since the measured capacitances varied little under these test conditions, we decided to evaluate the merit of the two reference capacitor structures in separate sensors in our first fabrication run.

3.3 Process Design

The manufacturing process of this sensor had two objectives. The first objective was to manufacture the capacitance measuring using the metal gate, P-well CMOS, (Complementary Metal Oxide Silicon), technology available in our facility. The second was to manufacture on the same substrate the capacitor structures discussed above.

In setting the processing step order, we considered the three dimensional geometry desired in the sensor and the compatibility of each processing step with high temperature processes. Obviously if aluminum metallization and polyimide were present on the wafer it could not be subjected to temperatures much greater than 450 °C. As a result of these considerations, the general order of processing was to fabricate the measuring circuitry on the substrate as a

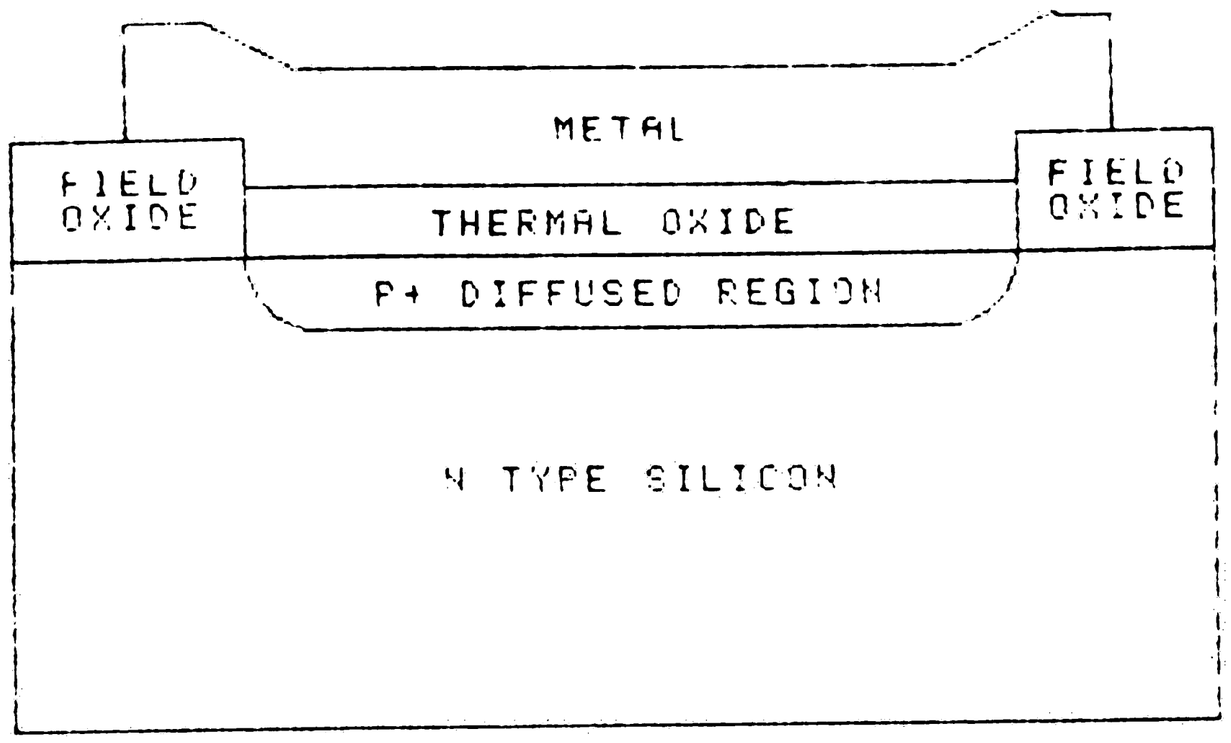


Figure 3-3: Reference Capacitor with Silicon Dioxide Dielectric

first step and the capacitor structures containing polyimide as a second general step. The exception here was that the bottom electrode, the P^+ diffused region, of every capacitor in the circuit is formed as part of the CMOS process. The reference capacitors with a thermal oxide dielectric are also formed in their entirety during the CMOS process.

The CMOS process steps were simulated with the process simulation, SUPREM, a resident program on Lehigh University's Cyber computer. An example of a SUPREM program is shown in Appendix B.

3.4 Layout

The circuit was laid out on the Applicon 860 VLSI Interactive Graphics System. After considerstion of our capabilities, we selected 5 microns for our design rule dimension, λ. λ is the smallest feature placed in the layout. All other features are based on that dimension. λ is usually chosen from a consideration of the technology available and the effects of geometry on the performance of the circuit. As it turns out, one text recommends limiting geometries to 5 microns or above to reduce noise in analog circuits [16].

Another layout consideration was what multiples of λ to assign to the photomask levels used to define the polyimide regions. Various polyimides were photolithographly processed with resolution test masks. The minimum polyimide dimension was set at 2λ as a result of our tests.

Appendix C shows the process function and design rules for each photomask level as a summary of the process design and layout.

Three circuits were combined on one chip for processing convenience. The first circuit consists of only the capacitance measuring circuit so that its function can be tested in isolation from the sensing element. The integrated sensor

with polyimide reference capacitors and the sensor with thermal silicon dioxide reference capacitors comprise the second and third circuits respectively.

The dimensions of the sensor and reference capacitors, C_x, C_o and C_{ref} were set so that the ratio of area to perimeter was kept the same for all three in keeping with good practice for circuits with ratioed capacitors. The areas of these capacitors were selected so that each sensor has an output span of from one to five volts for a range in relative humidity of 0 to 100% according to Equation (2.18).

3.5 Fabrication

Two process runs have been completed. The circuit was fabricated on MOS grade, n type, silicon substrates with a resistivity of 2-3 Ω-cm.. The CMOS processing presented few difficulties. Process results were monitored using spreading resistance, stylus film thickness, four point probe, and C-V measurement techniques.

We did encounter process difficulties in establishing good ohmic contact between metal layers through the polyimide vias. This is a well known problem in polyimide processing and we were able to solve the problem after reviewing the literature and using backsputtering of the lower metal layer before deposition of the upper metal layer [8]. The polyimide used for our process was Dupont's PI-2555 Pyralin. As explained in the next chapter, the control of the thickness of the polyimide became a critical factor for the sensor with silicon dioxide reference capacitors.

Chapter 4
Testing and Evaluation of Results

4.1 Testing

Testing of our completed integrated relative humidity sensors is in its infancy. Our primary measurement to date has been some preliminary measurements of the output of the sensor as it is exposed to different relative humidity environments.

The sensors were prepared for measurement by dicing the wafers and mounting the chips for test in ceramic DIPs, (Dual Inline Packages). After wire bonding, the DIP was covered with a ceramic cap that allowed air flow into the sensor but kept the chip from being exposed to light.

Each sensor package was placed in various relative humidity environments. This was accomplished by suspending the sensor above saturated salt solutions in closed containers. This technique makes use of the fact that the vapor pressure of water above a saturated aqueous salt solution in a closed container remains constant. Figure 4-1 shows a diagram of the apparatus. The temperature of each bath should be known as the relative humidity is temperature dependent. Table 4-1 shows the saturated salt solutions we used and their associated relative humidities. To simulate a dry environment, (close to 0% RH), the sensor was placed in a closed container with molecular sieve material that had been baked out. Leads were brought out to a Hewlett Packard 6114A Precision Power Supply and a Hewlett Packard 3468B Multimeter. The output voltage of the sensor was measured as a function of relative humidity.

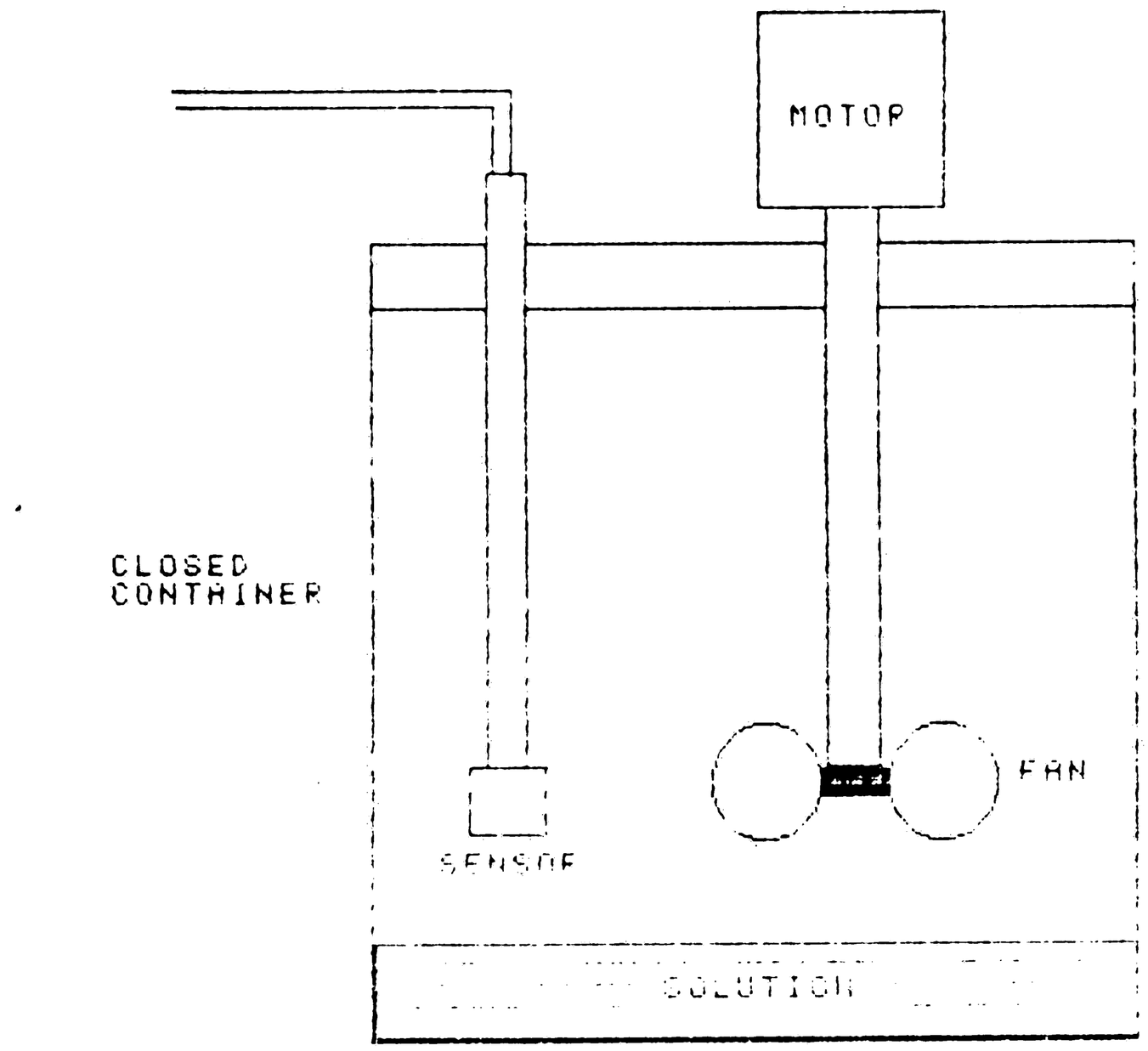


Figure 4-1: Saturated Salt Solution Apparatus

Salt Solution Humidity Standards	
Solution	**%RH at 25 °C**
Lithium Chloride	11.3
Magnesium Chloride	32.78
Magnesium Nitrate	52.89
Sodium Chloride	75.29
Potassium Chloride	84.34
Potassium Nitrate	93.58

Table 4-1: Relative Humidities of Various Saturated Salt Solutions

4.2 Results

The graphs in Figures 4-2 and 4-3 show the results of our measurements on two separate process runs of sensors with silicon dioxide reference capacitors (solid lines) as compared with our target output (dotted line). The large deviation of these solid curves can be explained by the examination of Equation (2.18) which I reproduce here.

$$V_{out}=\frac{C_x-C_o}{C_{ref}}V_{ref}$$

In Figure 4-2, the deviation can explained by the polyimide dielectric in C_x being too thick, hence making C_x too small and shifting the output curve down. Conversely the output of the sensor shown in Figure 4-3 reflects the fact that the polyimide dielectric in C_x is too thin.

The flattening of the curve in Figure 4-2 near 0% RH and of the curve in

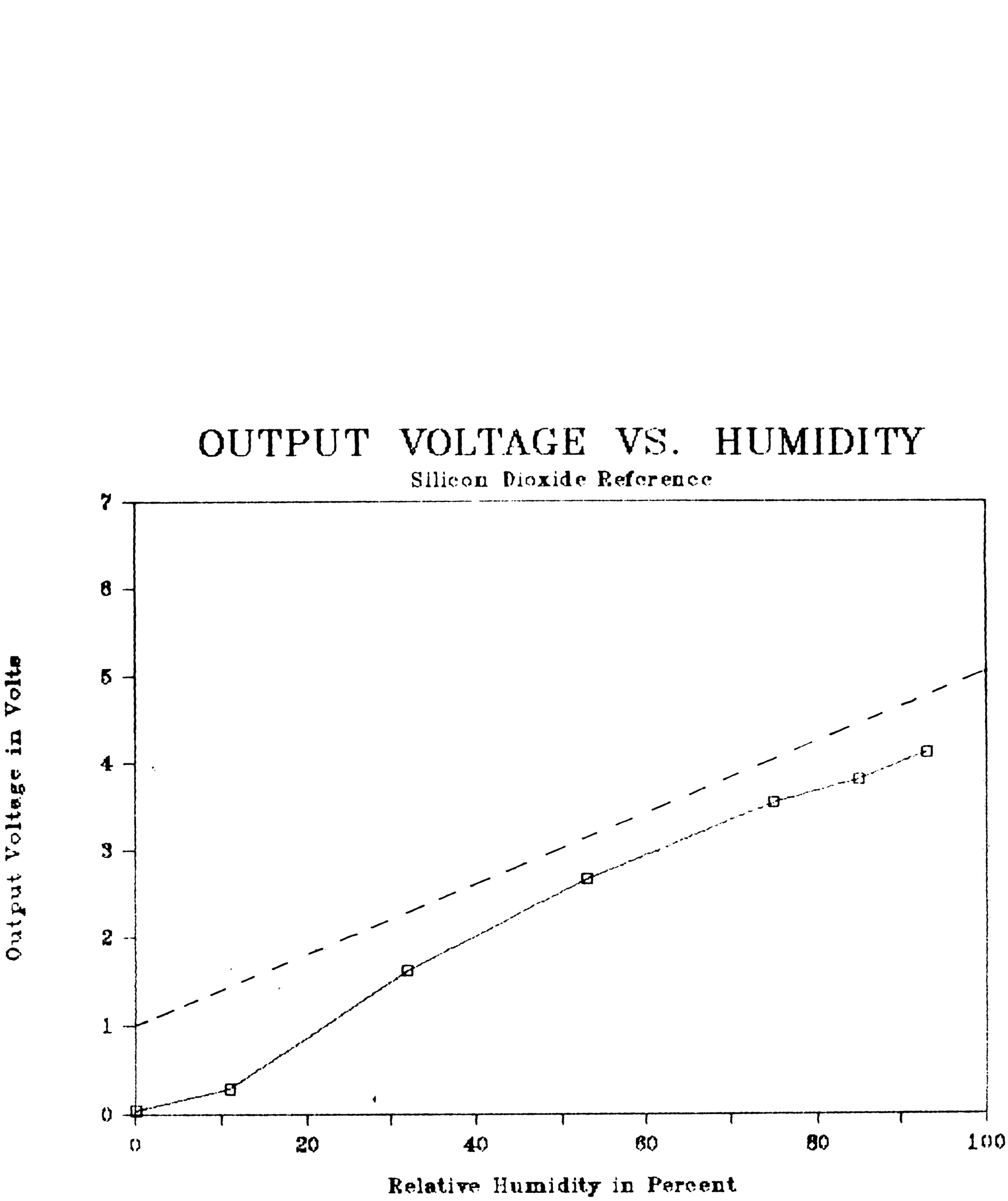


Figure 4-2: Measurement of the Output of a Silicon Dioxide Reference Capacitor Humidity Sensor, First Run

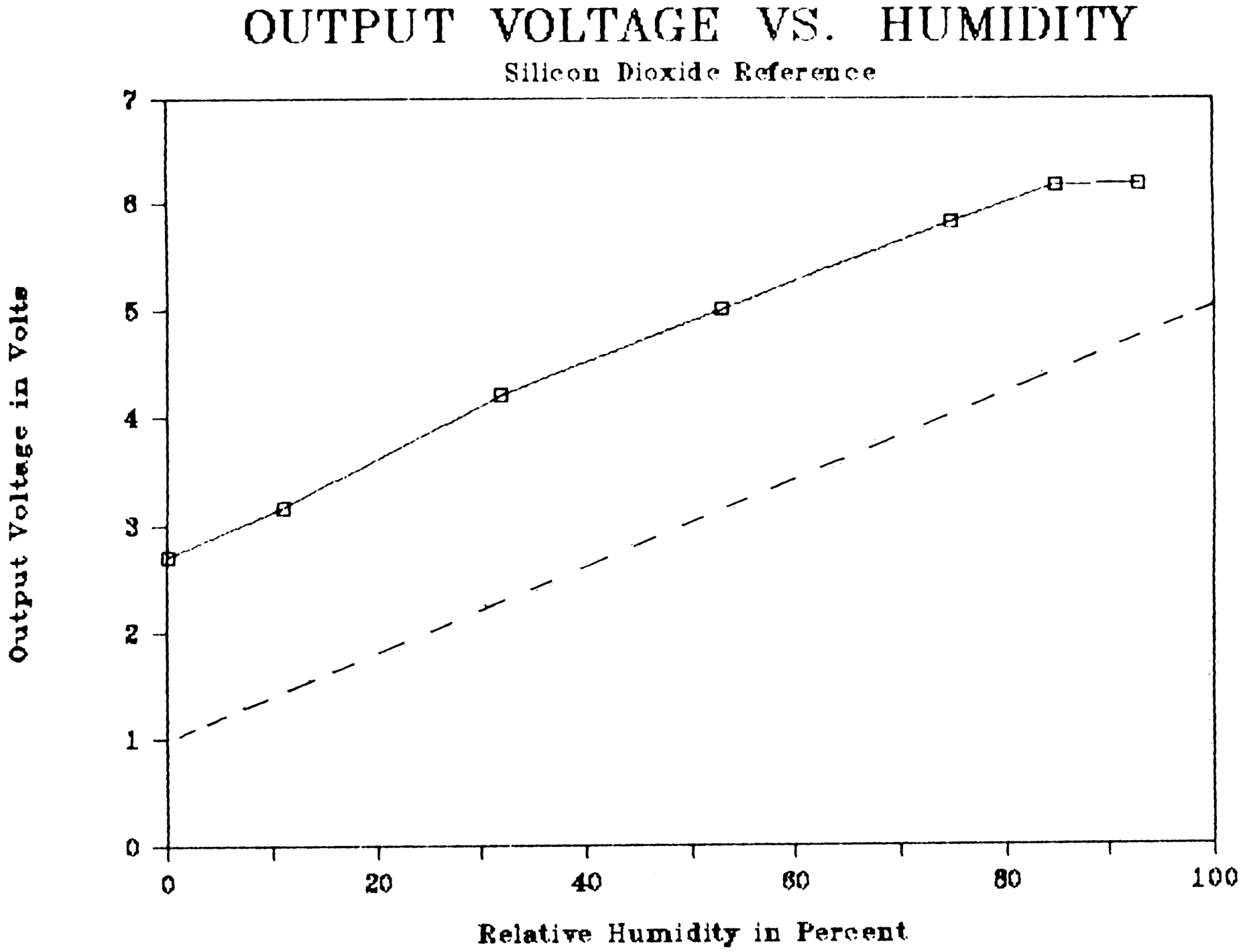


Figure 4-3: Measurement of the Output of a Silicon Dioxide Reference Capacitor Humidity Sensor, Second Run

Figure 4-3 near 100% RH reflects the fact that as a result of the offsets, the output voltage is approaching ground in one case and the power supply voltage in the other. The ideal output would be restricted to between 1 and 5 volts.

These results show how critical it is to control the relative thickness of the polyimide in C_x and the thermal oxide thickness in C_o and C_{ref} in the sensors with silicon dioxide reference capacitors. This critical need to control thickness is a disadvantage of this approach. The ratios of capacitances in the sensor with polyimide reference capacitors is controlled by the area of the capcitors alone in that the polyimide thickness across one chip should be fairly uniform. Allowing for this thickness problem the sensors with silicon dioxide reference capacitors seem to perform as expected.

The sensors which incorporate sealed polyimide dielectrics as reference capacitors showed indications that the reference capacitors were not effectively sealed from moisture permeation. When placed in high humidity environments, their output voltage tended to drop over a period of time. Looking again at Equation (2.18) one can see that if C_o and C_{ref} increase slowly because of moisture permeation the output will drop.

As an alternative we tried drying these polyimide reference capacitor sensors out between measurements at the various relative humidity environments in a kind of "pulsed" mode. When this was done, we had outputs shown in the graph in Figure 4-4. This result indicates that if the reference capacitors had been sealed the sensor would have performed close to target values.

The A.C. output of both devices was observed to measure the circuit's operation frequency and to verify the Integrator Stage's operation. Figure 4-5 shows a picture of the A.C. output. The photograph shows the typical action

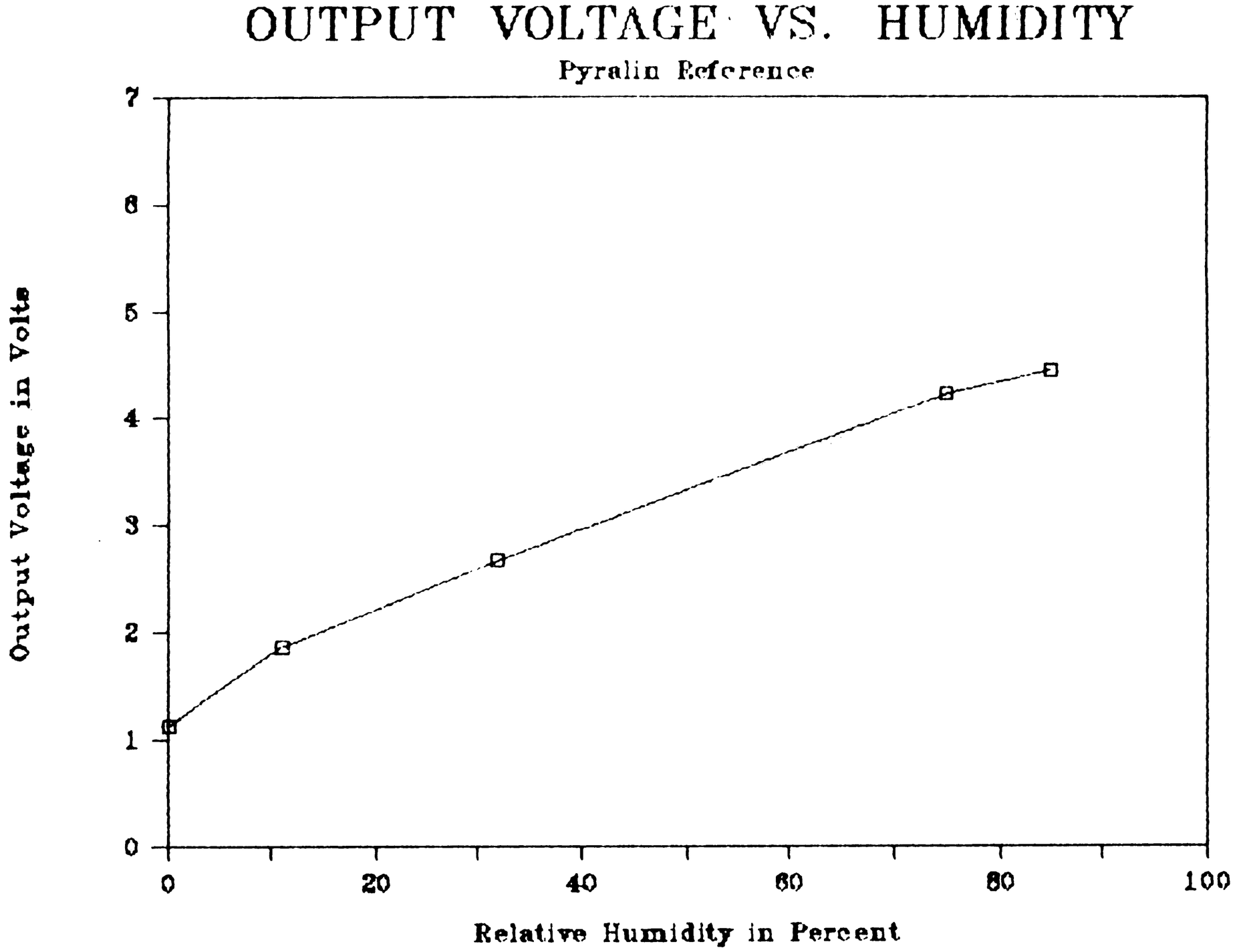


Figure 4-4: Output of the Sensor with Polyimide Reference Capacitors When Measured in "Pulsed" Mode

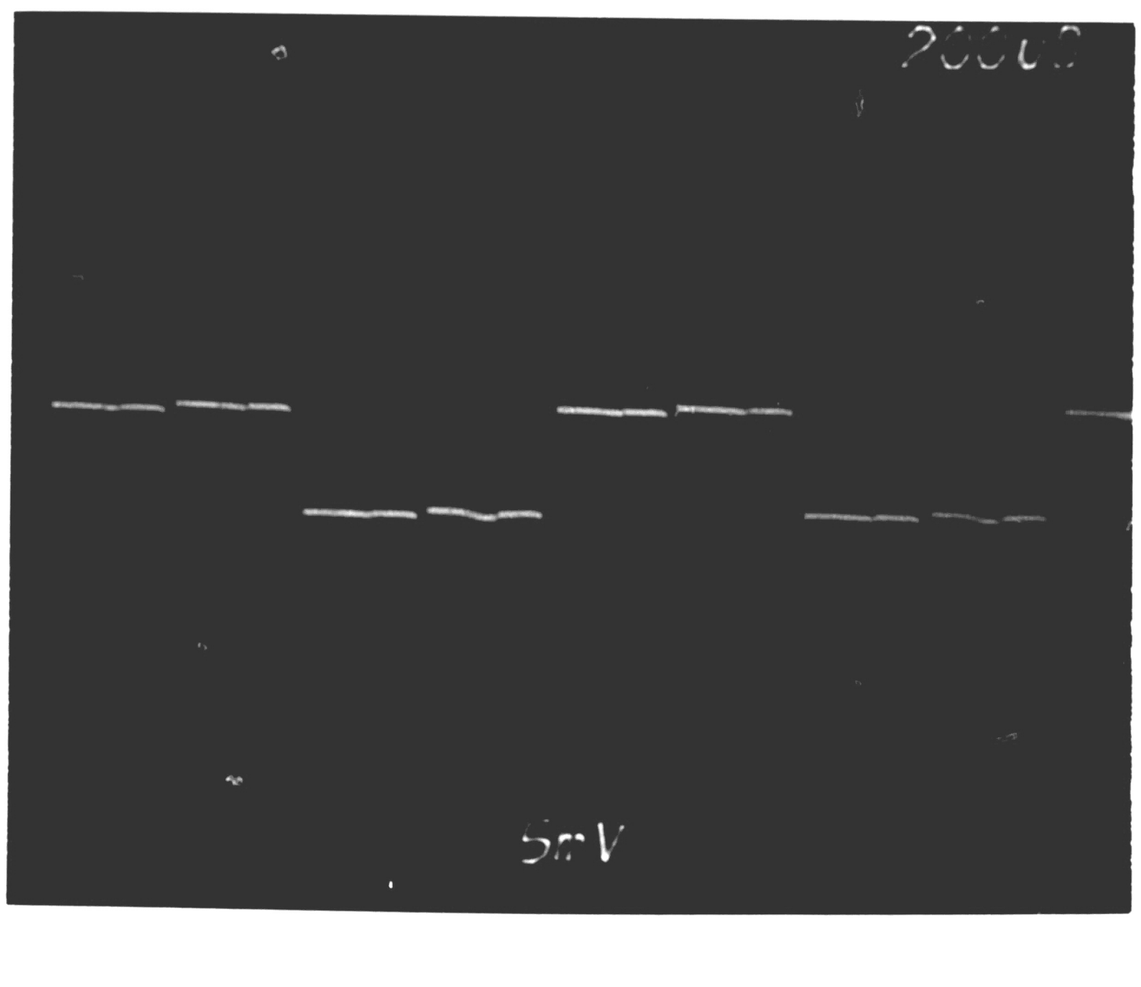


Figure 4-5: A.C. Output of the Sensor

of the integrator when the circuit is at balance. The output voltage is being stepped alternately above and below the D.C. level.

Work continues in attempts to measure linearity, hysteresis, response time and repeatability of the sensors. Additional wafers are being processed in an attempt to correct the process difficulties encountered.

4.3 Conclusions

We have demonstrated to some extent that a humidity measuring capacitive sensor and a signal processing circuit using switched capacitor techniques can be synthesized on the same silicon substrate. The design using the silicon dioxide reference capacitors seems to be the most promising for use as a practical sensor in the near term in that its shortcomings can probably be improved with better process control. The design using the polyimide structure shows a more fundamental structure problem that will be more difficult to correct.

4.4 Recommendations

There are 4 areas where more work needs to be done.

1. The existing sensor with silicon dioxide reference capacitors needs to be fully characterized. Characteristics like response time, linearity, repeatibility, etc. need to be determined. Ways to improve the processing in order to achieve better accuracy in capacitor values should be investigated.

2. Ways to effect better moisture seals on the reference capacitors of the polyimide reference sensor could be investigated as this design shows some promise.

3. The characteristics of the sensing element itself should be investigated to see how it differs from its descrete relatives.

4. The incorporation of additional on-board circuit functions, such as temperature compensation and linearity correction, could be investigated.

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Appendix A
Two Phase Non-Overlapping Clock

A.1 General Circuit

Figure A-1 shows a conceptual diagram of the clock circuit. It consists of three parts, a multivibrator, a D flip-flop and a logic circuit to convert the output of the flip-flop to a two phase non-overlapping clock.

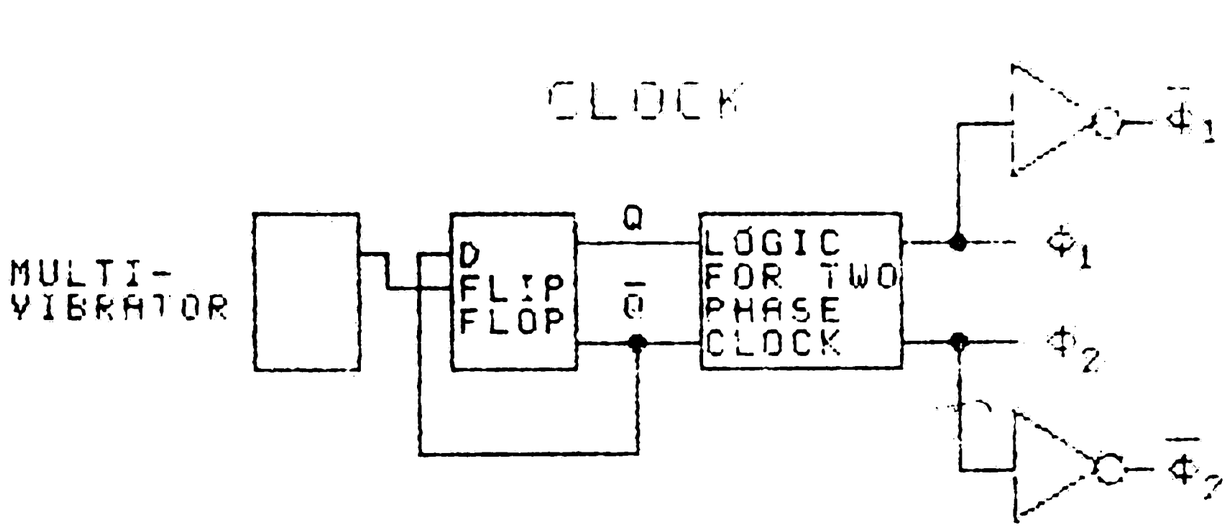


Figure A-1: Non-Overlapping Clock Circuit

A.2 Multivibrator

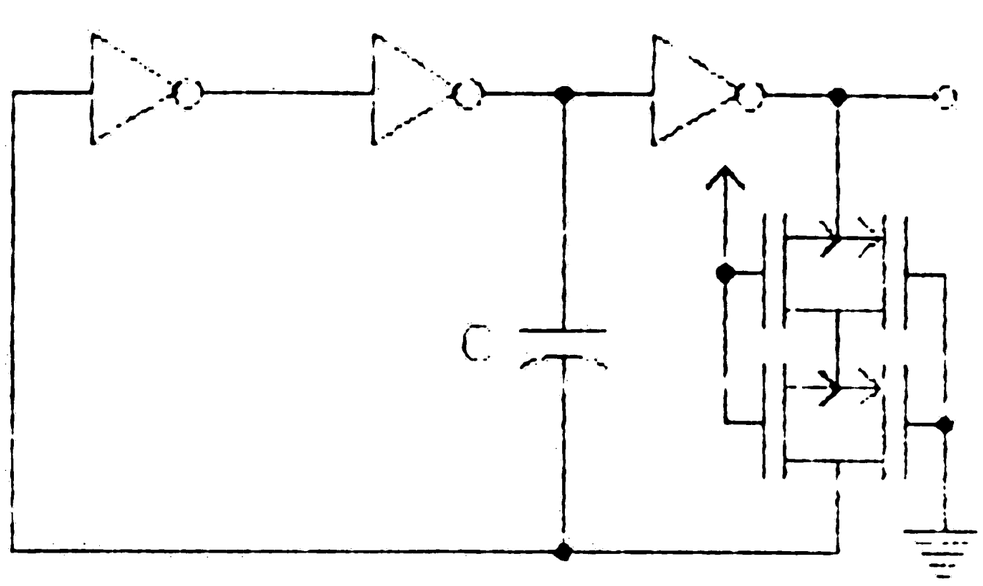
Figure A-2(a) shows the multivibrator subcircuit whose function is to generate a square wave. It consists of three cascaded invertors whose output is fed back to its input through two transmission gates. The gates of the transistors of the transmision gates are set so that they are always on. This means that the transmission gates together act as a resistor. An equivalent circuit is shown in Figure A-2(b) The addition of the capacitor sets the frequency, f of the output at $f=\frac{1}{RC2\ln 2}$ where C is the capacitance and R is the equivalent resistance of the transmission gates.

A.3 D Flip-Flop

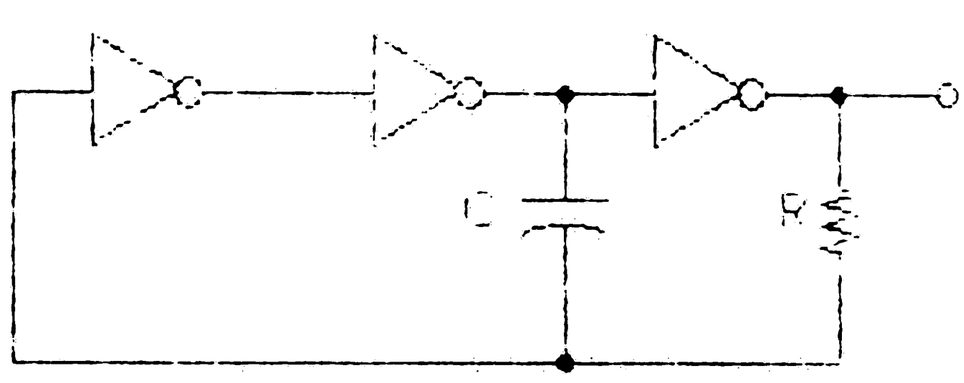
Figure A-3 shows a conventional CMOS implementation of a D flip-flop as it is set up in this circuit. The purpose of the flip-flop as it used here is to sharpen the output of the multivibrator and to counteract any unevenness in the half cycles of the multivibrator output by dividing the frequency in two. It provides two outputs Q and $\overline{Q}$ to the suceeding logic stage.

A.4 Logic Stage

This stage is shown in Figure A-4. The function of this stage is to take the two outputs from the D flip-flop, Q and $\overline{Q}$ and convert them into two clock phases. The circuit uses the fact that each gate has a propagation delay which is the time period that elapses before a change in a gate's input is reflected at its output. Table A-1 shows the state of each of the nodes of the circuit as traverses through one cycle. Figure A-5 shows the resulting clock signals.



(a)



(b)

Figure A-2: Multivibrator Circuit, (a) Actual Circuit, (b) Equivalent Circuit

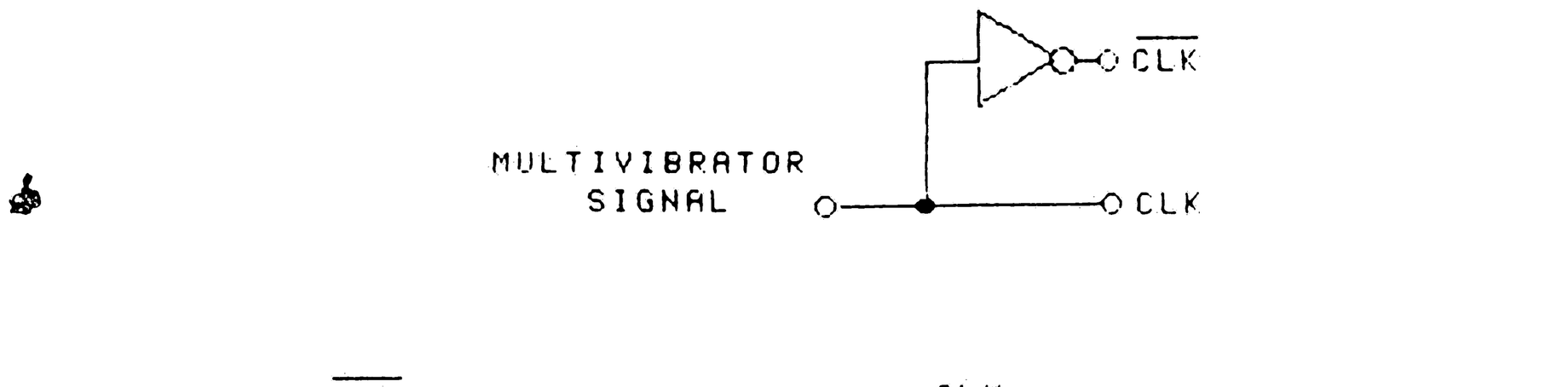


Figure A-3: D Flip-flop

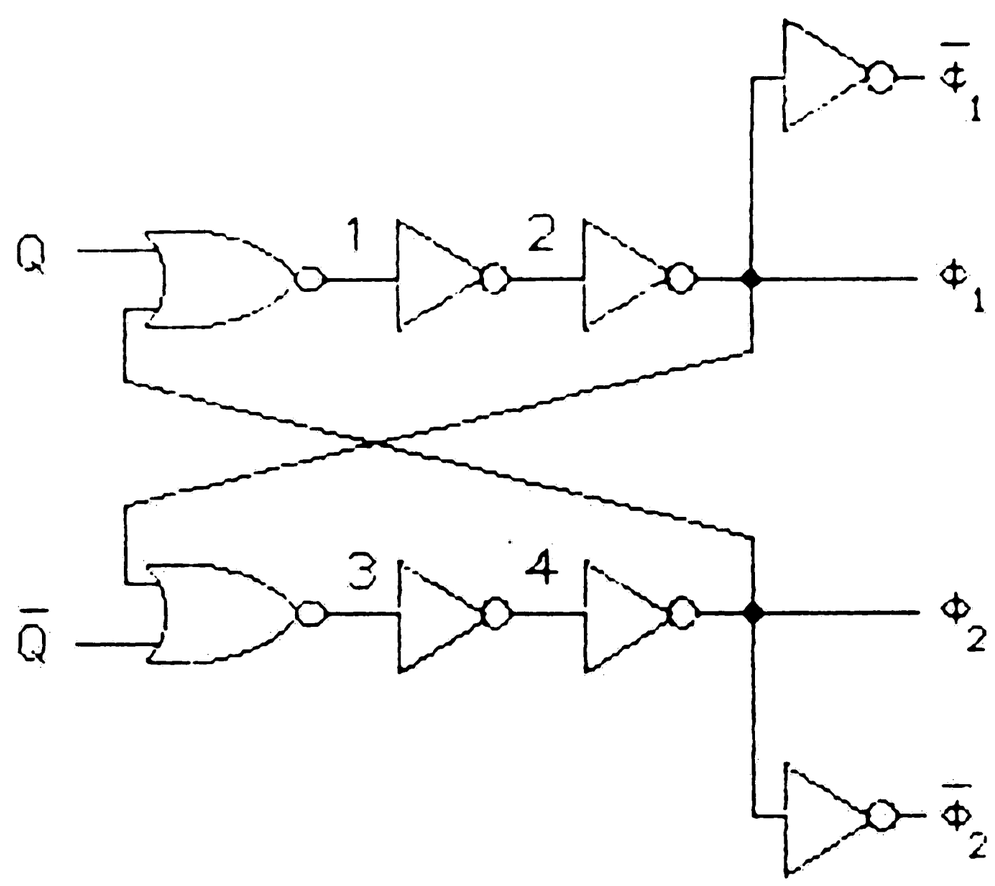


Figure A-4: Logic to Create Two Phase Non-Overlapping Clock

POINT IN CYCLE	NODES							
	Q	$\overline{Q}$	1	2	3	4	Φ_1	Φ_2
MIDDLE OF FIRST HALF CYCLE	1	0	0	1	1	0	0	1
HALF CYCLE END	0	1	0	1	1	0	0	1
AFTER FIRST GATE DELAY	0	1	0	1	0	0	0	1
AFTER SECOND GATE DELAY	0	1	0	1	0	1	0	1
AFTER THIRD GATE DELAY	0	1	0	1	0	1	0	0
AFTER FOURTH GATE DELAY	0	1	1	1	0	1	0	0
AFTER FIFTH GATE DELAY	0	1	1	0	0	1	0	0
MIDDLE OF SECOND HALF CYCLE	0	1	1	0	0	1	1	0
SECOND HALF CYCLE END	1	0	1	0	0	1	1	0
AFTER FIRST GATE DELAY	1	0	0	0	0	1	1	0
AFTER SECOND GATE DELAY	1	0	0	1	0	1	1	0
AFTER THIRD GATE DELAY	1	0	0	1	0	1	0	0
AFTER FOURTH GATE DELAY	1	0	0	1	1	1	0	0
AFTER FIFTH GATE DELAY	1	0	0	1	1	0	0	0
RETURN TO ORIGNAL STATE	1	0	0	1	1	0	0	1

Table A-1: State of Nodes of Two Phase Clock Generating Circuit During 1 Cycle

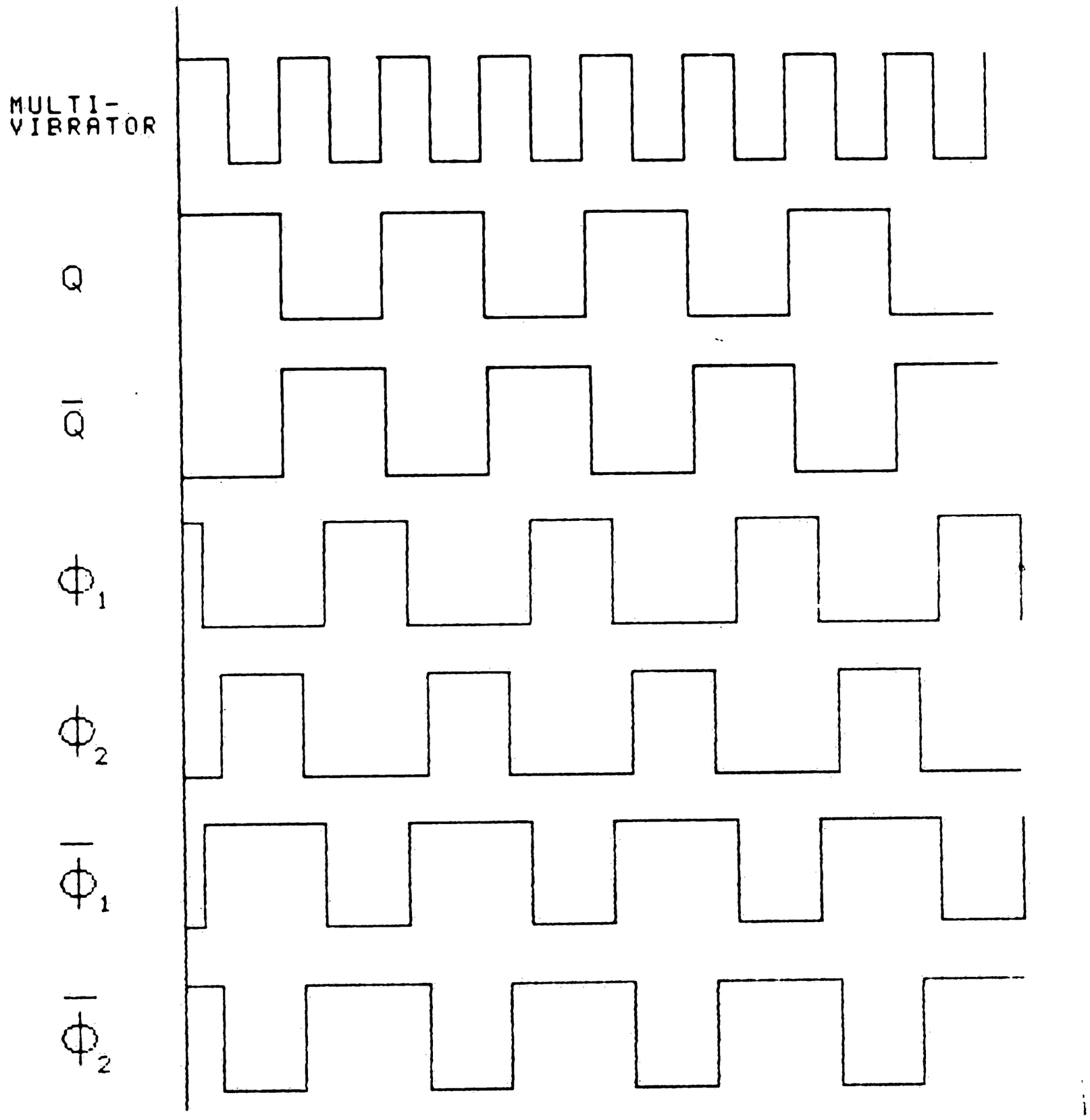


Figure A-5: Clock Signals of the Two Phase Non-Overlapping Clock

Appendix B
Example of SUPREM

Shown below is an example of a SUPREM program to model a phosphorus doping operation.

```
100 TITL PHOSPHORUS PREDEP CHARACTERIZATION
110 GRID YMAX=10
120 SUBS ORNT=100, ELEM=+, CONC=5E10
130 PRINT HEAD=Y
140 COMM PHOSPHORUS PREDEP
150 MODEL NAME=MPH1, DSXN=7E10
160 STEP TYPE=PDEP, ELEM=P, CONC=7E19, TIME=30, TEMP=850, MODL=MPH1
170 END
```

Appendix C
A List of the Process Function and Layout for Each Mask Level

1. First Photomask Level.

   a. Functions.

      i. Define P^- well regions.

      ii. Define diffusion resistors.

   b. Design Rules.

      i. Minimum distance from unrelated diffusion area, 5λ.

      ii. Minimum feature width, 2λ.

      iii. Guard ring overlap, 3λ.

2. Second Photomask Level.

   a. Functions.

      i. Define source and drains on PMOS transistors.

      ii. Define guard ring on P^- well regions.

      iii. Define lower plate on capacitors.

      iv. Provide conductors across metal lines.

      v. Provide contact to P^- well regions.

      vi. Define diffusion resistors.

   b. Design rules.

      i. Minimum distance from unrelated diffusion area, 3λ.

ii. Minimum feature width, 2λ.

3. Third Photomask Level.

a. Functions.

i. Define source and drains on NMOS transistors.

ii. Provide contact to substrate.

iii. Define diffusion resistor.

iv. Define scribe lines.

b. Design rules.

i. Minimum distance from unrelated diffusion area, 3λ.

ii. Minimum feature width, 2λ.

4. Fourth Photomask Level.

a. Functions.

i. Define gate windows.

ii. Define contact windows.

iii. Define capacitor dielectric.

b. Design rules - Minimum feature dimension, 2λ.

5. Fifth Photomask Level.

a. Functions - redefine contact windows.

b. Design rules - Minimum feature dimension, 2λ.

6. Sixth Photomask Level.

a. Functions.

i. Define metal circuit connections.

ii. Define metal gates.

iii. Define metal contacts.

iv. Define bonding pads.

v. Define top plate to oxide capacitor.

b. Design rules.

i. Minimum distance from unrelated metal line, 3λ.

ii. Minimum feature width, 3λ.

7. Seventh Photomask Level.

a. Functions - open field oxide for polyimide dielectric.

b. Design rules - no special design rules, all overlaps 1 λ.

8. Eighth Photomask Level.

a. Functions.

i. Define polyimide dielectric for capacitors.

ii. Define polyimide passivaton for measuring circuit.

b. Design rules.

i. Minimum overlap of field oxide, 2λ.

ii. Minimum feature separation, 5λ.

iii. Minimum separation from scribe line, 5λ

9. Ninth Photomask Level.

a. Functions.

i. Define upper plate on polyimide reference capacitors.

ii. Define additional bonding pad layer.

b. Design rules.

i. Minimum distance from unrelated metal line, 3λ.

ii. Minimum feature width, 3λ.

10. Tenth Photomask Level.

a. Function - Define upper conductive mesh on sensor.

b. Design rules - no special design rules, all overlaps 1 λ.

11. Eleventh Photomask Level.

a. Functions.

i. Define top polyimide layer on sensor.

ii. Define an additonal passivation layer for measuring circuit.

b. Design rules.

i. Minimum feature separation, 5λ.

ii. Minimum separation from scribe line, 5λ

All other dimensions have a minimum of 1λ. "

Vita

Spencer Silverthorne was born in Bronxville, N.Y. to Spencer V. and Holly A. Silverthorne. He attended Villanova University and received a Bachelor of Science degree in Physics in 1973. He is presently a member of the Solid State Group of the research department of Leeds and Northrup Instruments Co. .